

Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

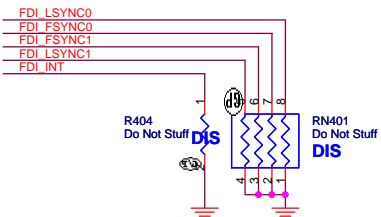
Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

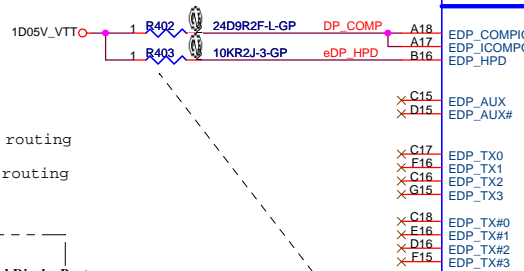
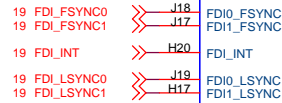
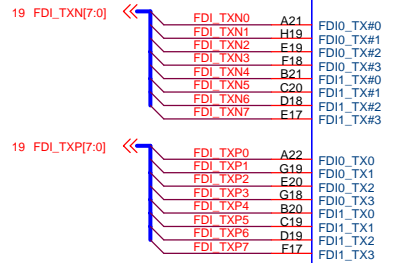
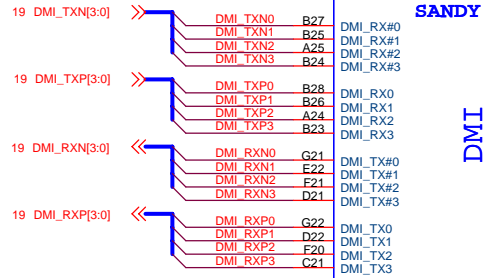
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics
function for power saving.

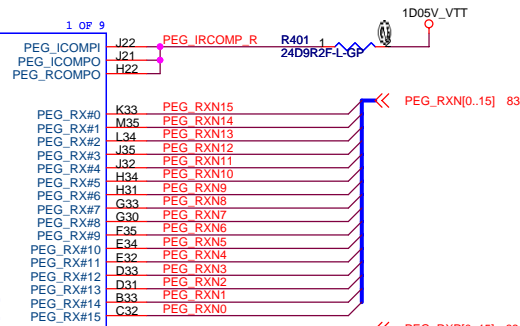


CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821



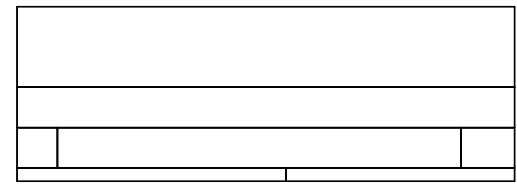
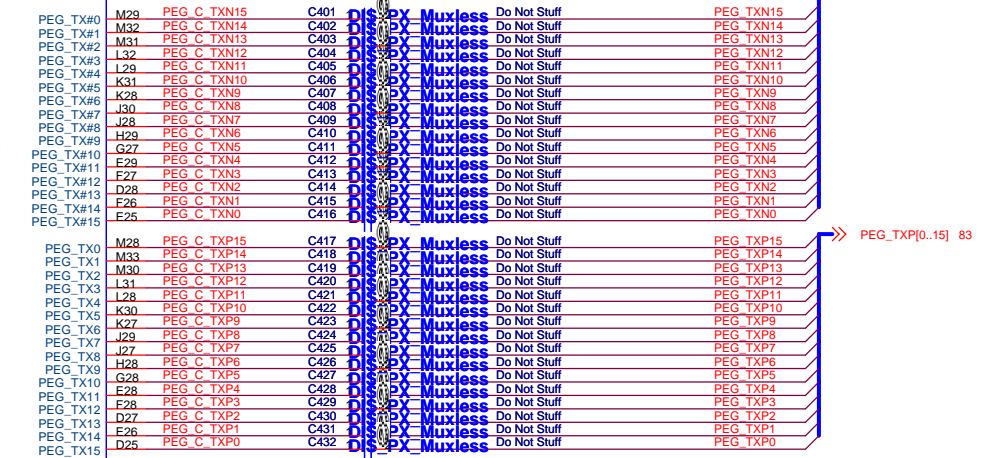
NOTE:
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns. If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up
resistor on the motherboard.

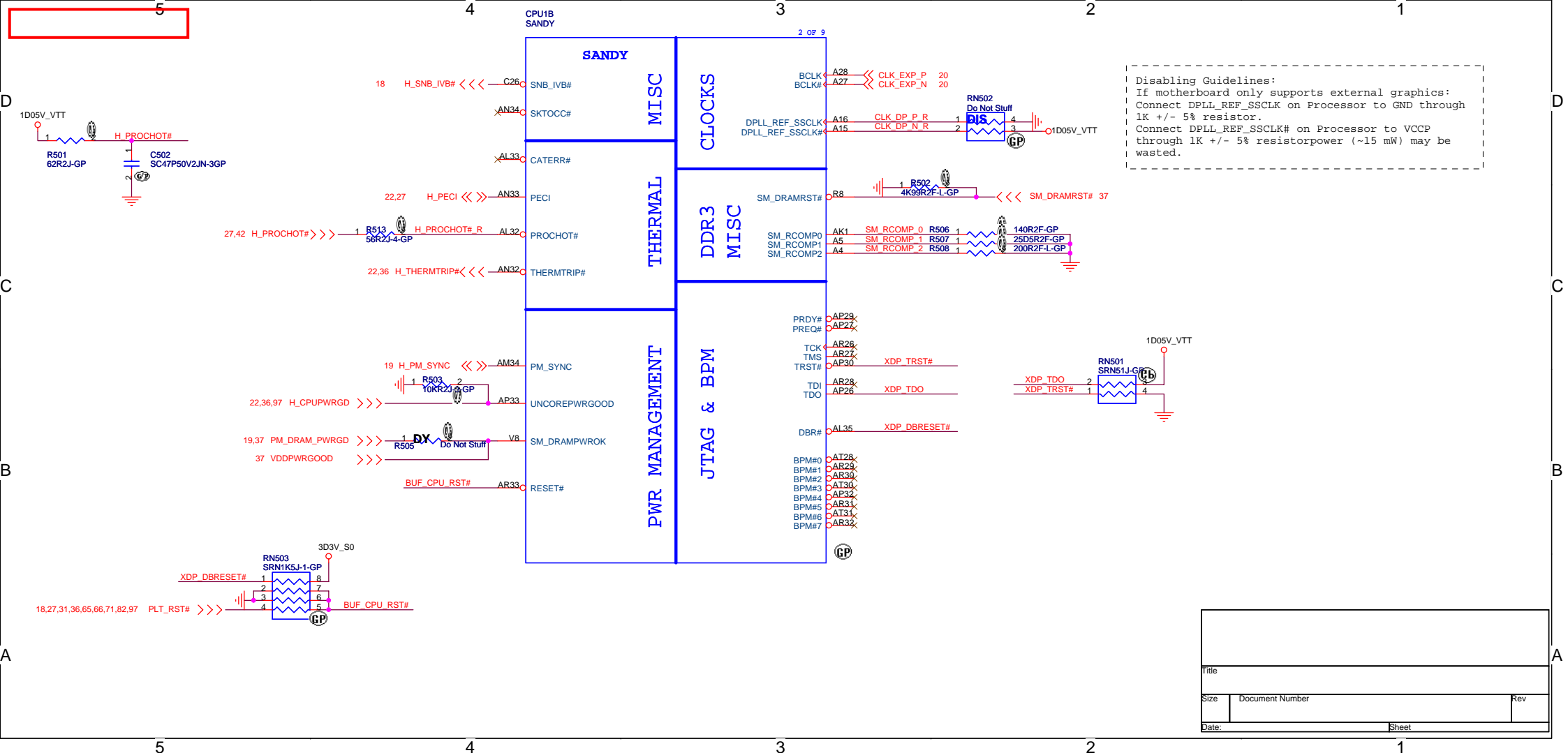
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

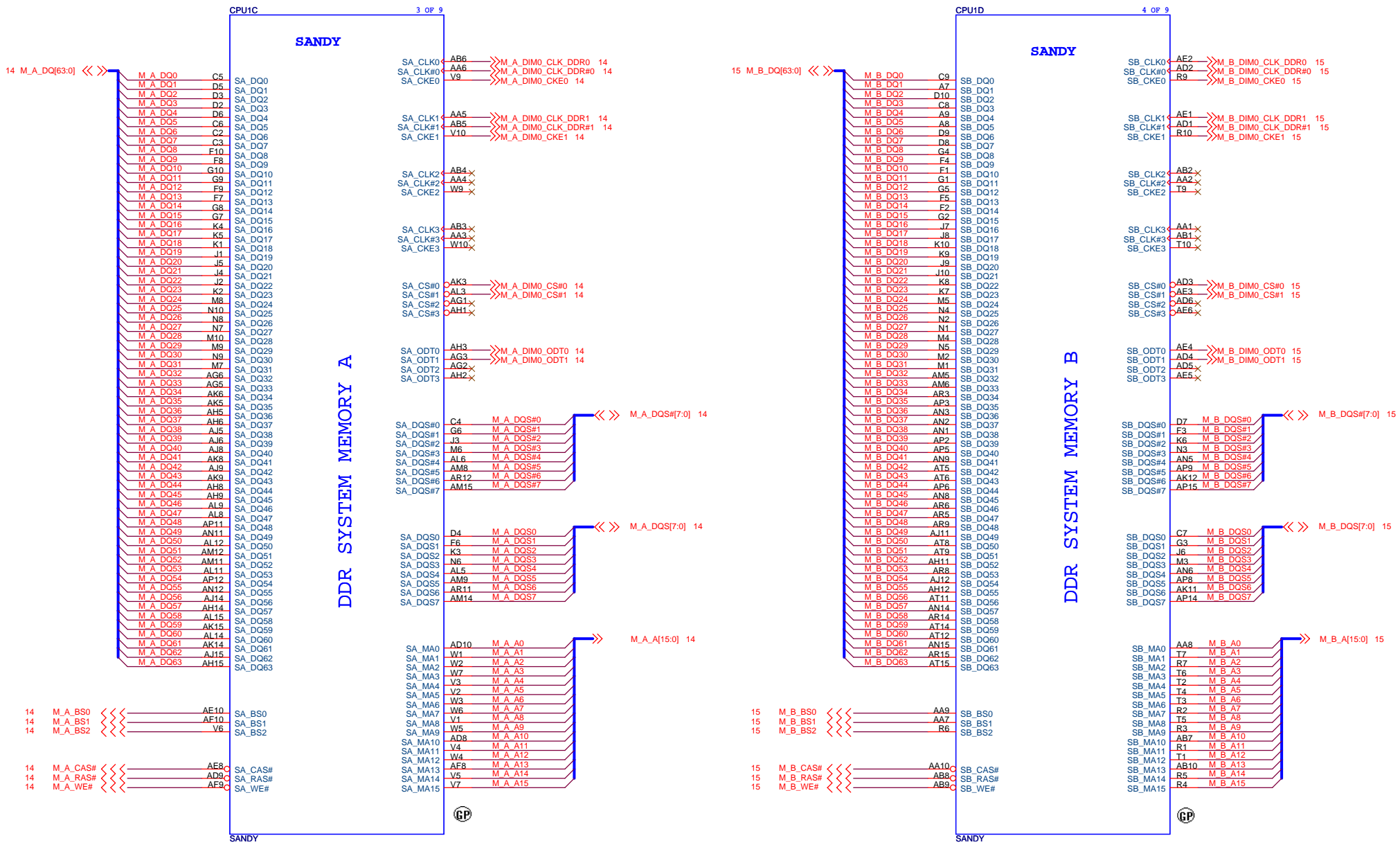


NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal





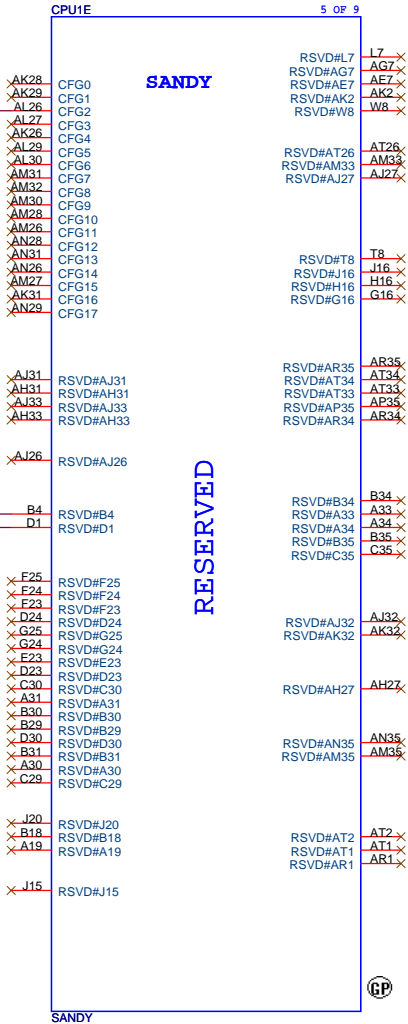
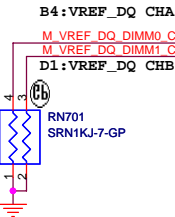


Title		
Size	Document Number	Rev
Date:	Sheet	



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

DIS_PX_Muxless

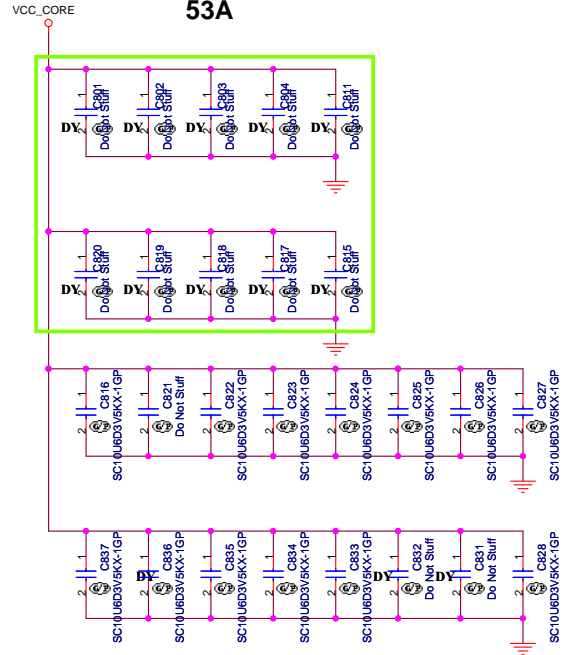


Title		
Size	Document Number	Rev
Date:	Sheet	

POWER

PROCESSOR CORE POWER

53A



VCC_CORE

SANDY

AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AF35 VCC
AF34 VCC
AF33 VCC
AF32 VCC
AF31 VCC
AF30 VCC
AF29 VCC
AF28 VCC
AF27 VCC
AF26 VCC
AD35 VCC
AD34 VCC
AD33 VCC
AD32 VCC
AD31 VCC
AD30 VCC
AD29 VCC
AD28 VCC
AD27 VCC
AD26 VCC
AC35 VCC
AC34 VCC
AC33 VCC
AC32 VCC
AC31 VCC
AC30 VCC
AC29 VCC
AC28 VCC
AC27 VCC
AC26 VCC
AA35 VCC
AA34 VCC
AA33 VCC
AA32 VCC
AA31 VCC
AA30 VCC
AA29 VCC
AA28 VCC
AA27 VCC
AA26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
Y32 VCC
Y31 VCC
Y30 VCC
Y29 VCC
Y28 VCC
Y27 VCC
Y26 VCC
V34 VCC
V33 VCC
V32 VCC
V31 VCC
V30 VCC
V29 VCC
V28 VCC
V27 VCC
V26 VCC
U35 VCC
U34 VCC
U33 VCC
U32 VCC
U31 VCC
U30 VCC
U29 VCC
U28 VCC
U27 VCC
U26 VCC
R35 VCC
R34 VCC
R33 VCC
R32 VCC
R31 VCC
R30 VCC
R29 VCC
R28 VCC
R27 VCC
R26 VCC
R25 VCC
P35 VCC
P34 VCC
P33 VCC
P32 VCC
P31 VCC
P30 VCC
P29 VCC
P28 VCC
P27 VCC
P26 VCC

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VIDALERT# AJ29 H_CPU_SVIDALRT# 1 R803 43R2J-GP << VR_SVID_ALERT# 42
VIDSCLK# AJ30 >>> H_CPU_SVIDCLK 42
VIDSOUT AJ28 >>> H_CPU_SVIDDAT 42

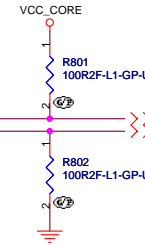
For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

H_CPU_SVIDDAT R804 1 130R2F-1-GP

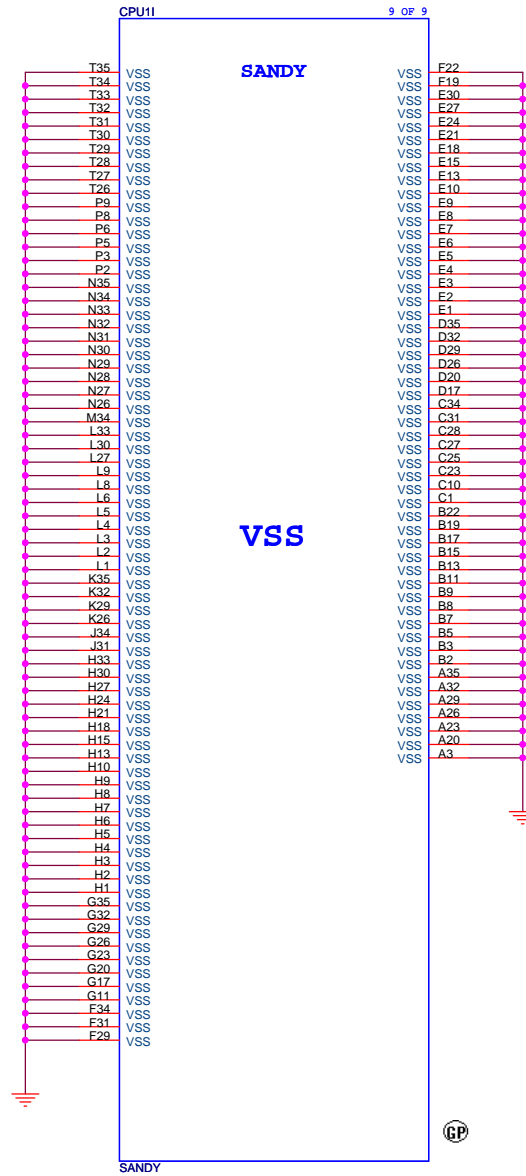
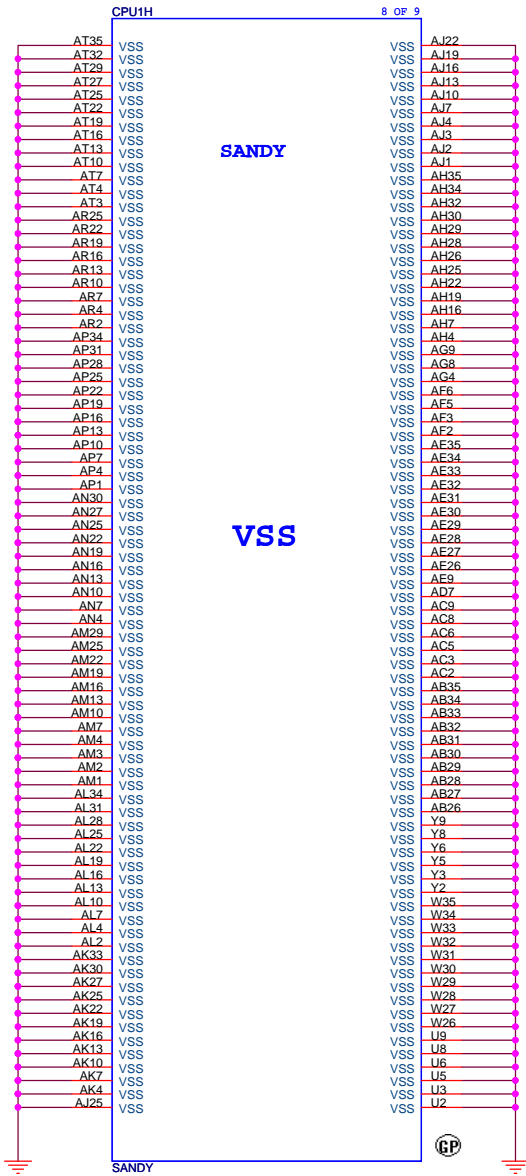
VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSSIO_SENSE

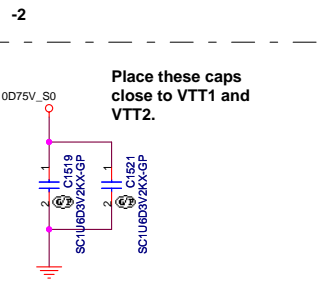
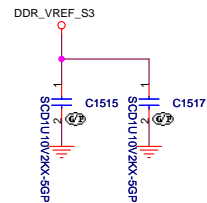
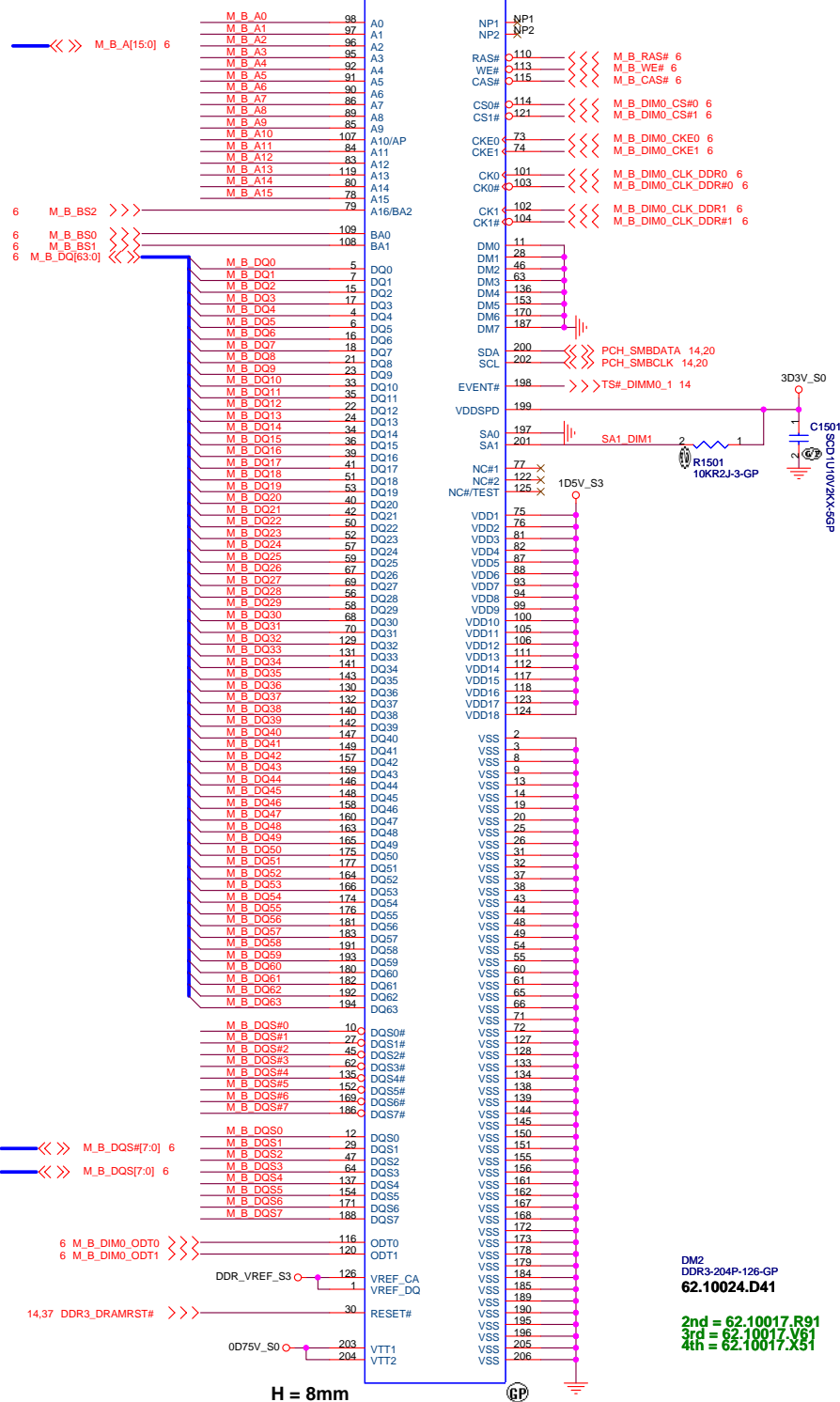
GP



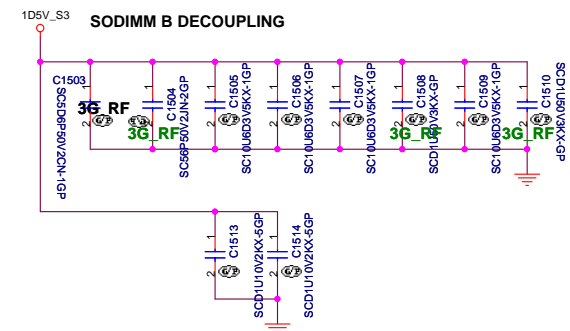
Title		
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Date:	Sheet	



SSID = MEMORY



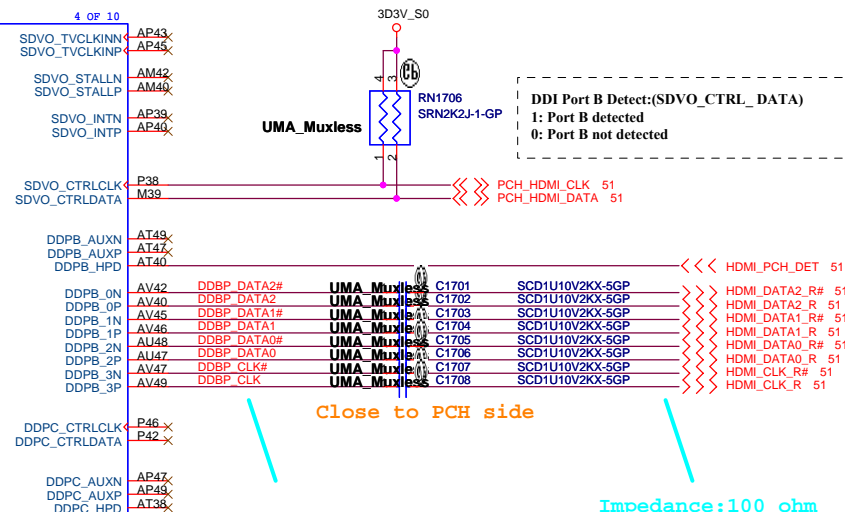
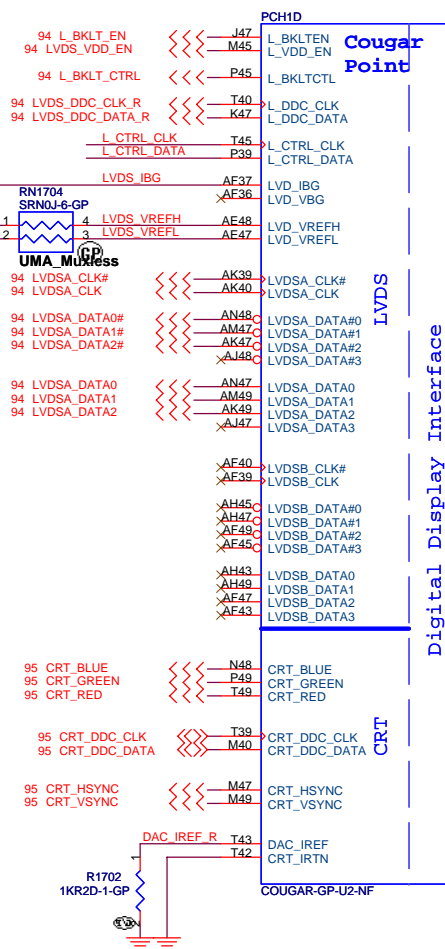
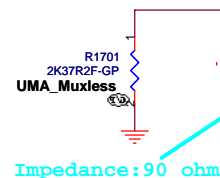
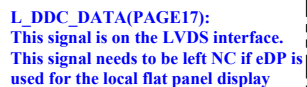
Layout Note:
Place these Caps near
SO-DIMMB.



DM2
DDR3-204P-126-GP
62.10024.D41

2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51

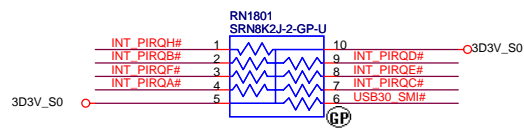
Title		
Size	Document Number	Rev
Date:	Sheet	



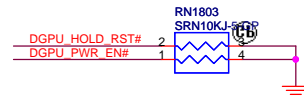
Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_0]P	SDVO_RED	DDPB_0]P	TMDSB_DATA2
	DDPB_0]N	SDVO_RED#	DDPB_0]N	TMDSB_DATA2#
	DDPB_1]P	SDVO_GREEN	DDPB_1]P	TMDSB_DATA1
	DDPB_1]N	SDVO_GREEN#	DDPB_1]N	TMDSB_DATA1#
	DDPB_2]P	SDVO_BLUE	DDPB_2]P	TMDSB_DATA0
	DDPB_2]N	SDVO_BLUE#	DDPB_2]N	TMDSB_DATA0#
	DDPB_3]P	SDVO_CLK	DDPB_3]P	TMDSB_CLK
	DDPB_3]N	SDVO_CLK#	DDPB_3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMI_B_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMI_B_CTRLCLK
SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMI_B_CTRLDATA	

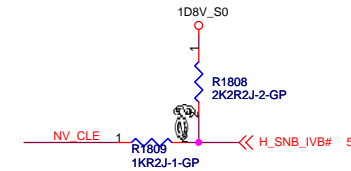
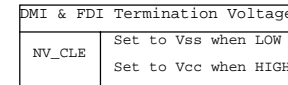
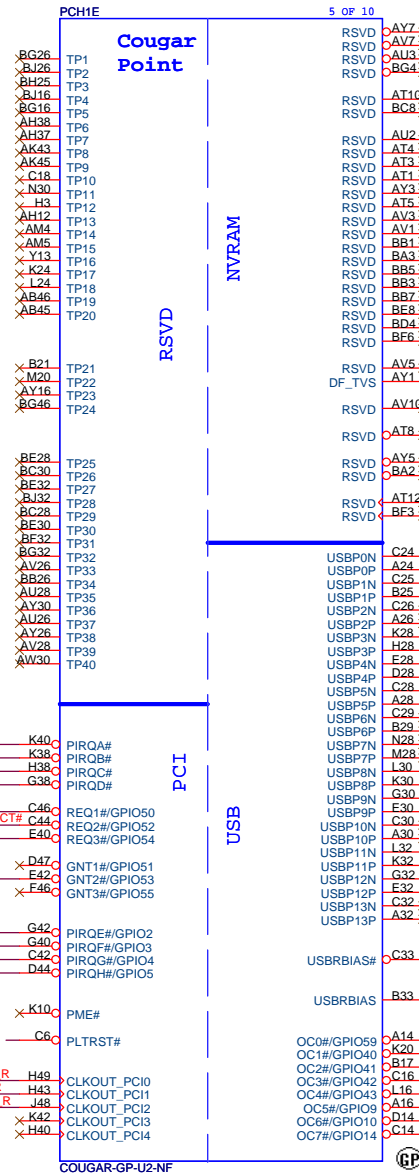
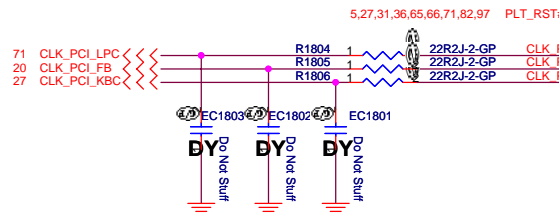
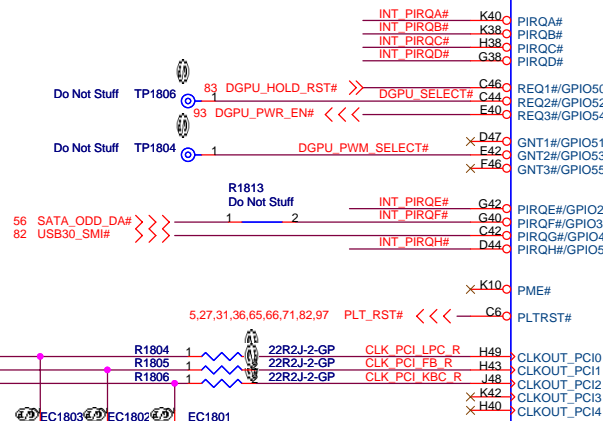
SSID = PCH



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
		SPI(Default)



- 2x USB Ext. port 1 (HS)
- x External debug port use on Huron river platform

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB C
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

Title		
Size	Document Number	Rev
Date:	Sheet	

SSID = PCH

4 DMI_RXN[3:0] <<<>>> 4
4 DMI_RXP[3:0] <<<>>> 4
4 DMI_TXN[3:0] <<<>>> 4
4 DMI_TXP[3:0] <<<>>> 4

FDI_TXN[7:0] 4
FDI_TXP[7:0] 4

Deep S4/S5 Supported

Deep S4/S5 Not Supported

VccDSW3_3

DPWROK

VccSUS3_3

RSMRST#

PCHIC

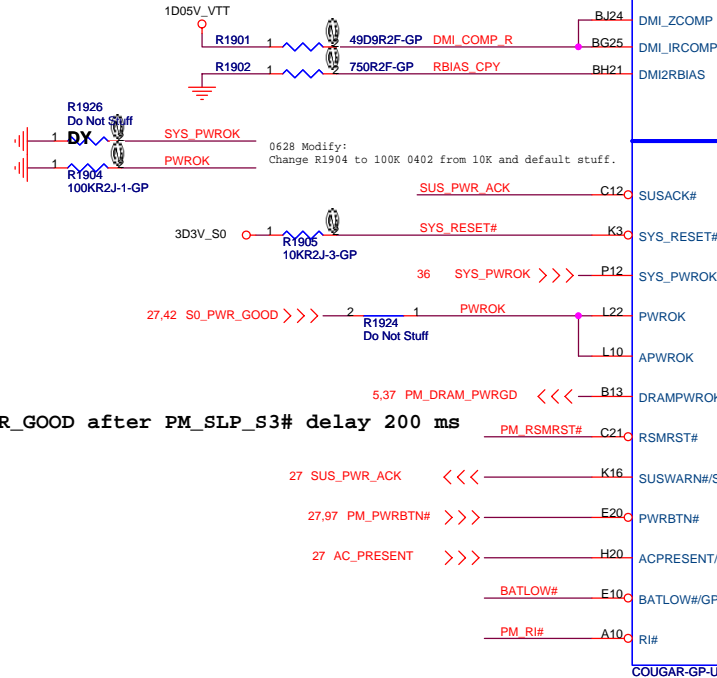
3 OF 10

Cougar
Point

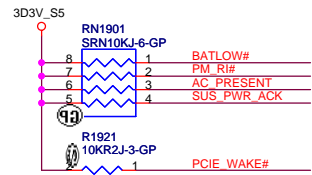
DMI

FDI

System Power Management

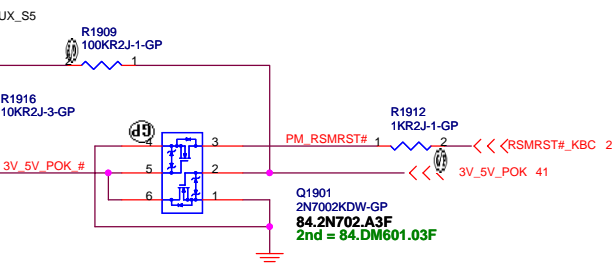


S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



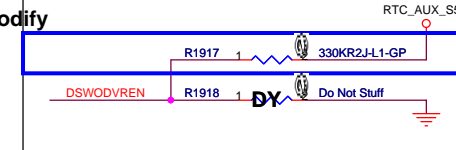
PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTTN#
This signal has an internal pull-up resistor

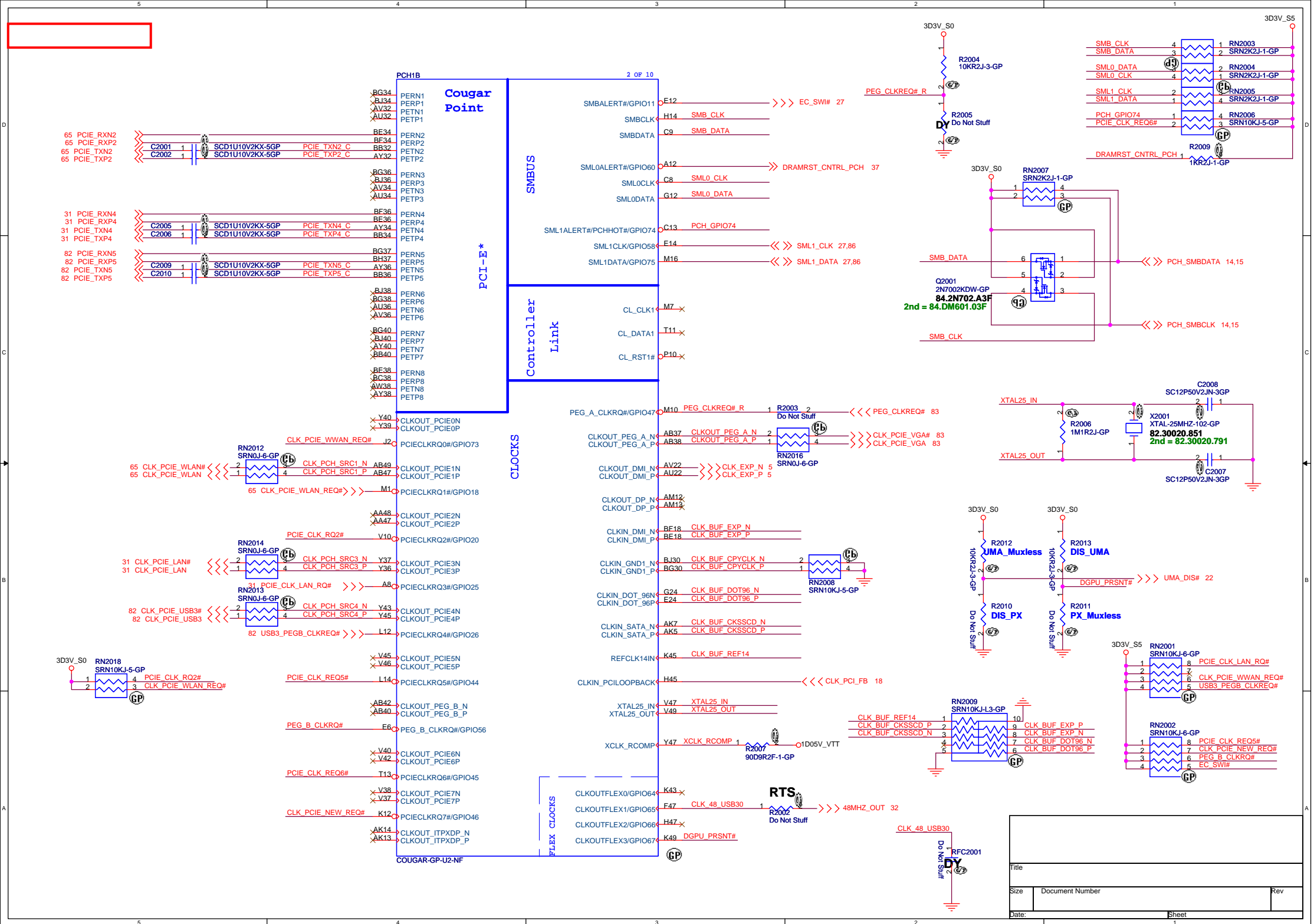


DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify



Title		
Size	Document Number	Rev
Date:	Sheet	

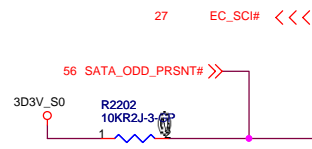
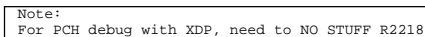



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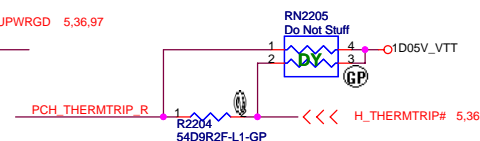
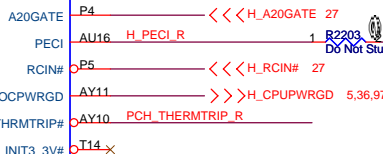
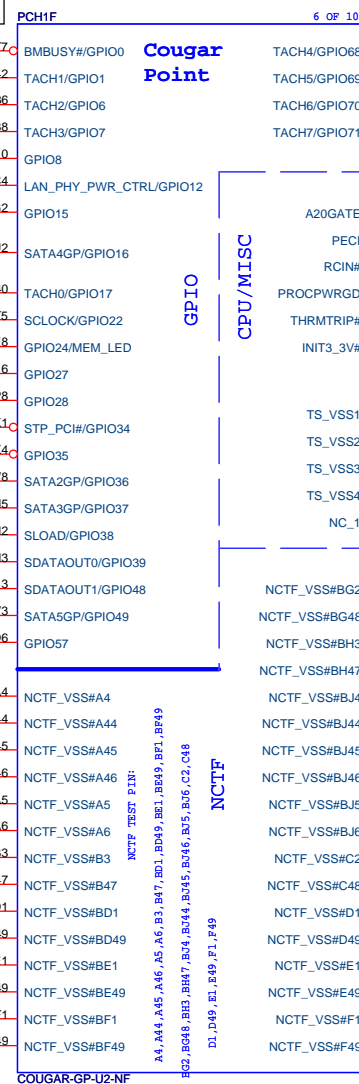
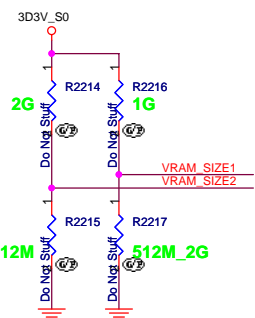
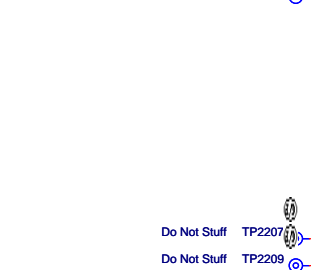
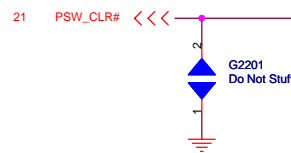


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21 PSW CLR# <<<< 



TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

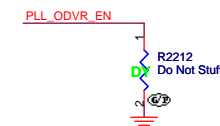
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved
via soft-strap. The default is integrated clock
enable.

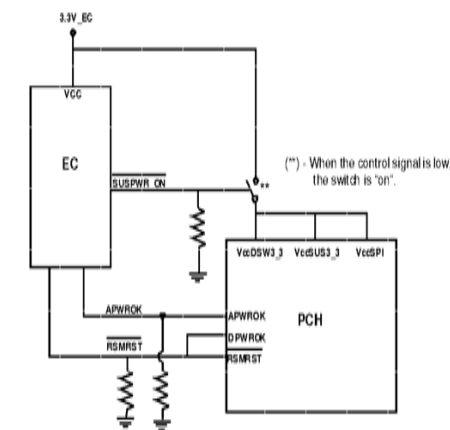
PLL ON DIE VR ENABLE

NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

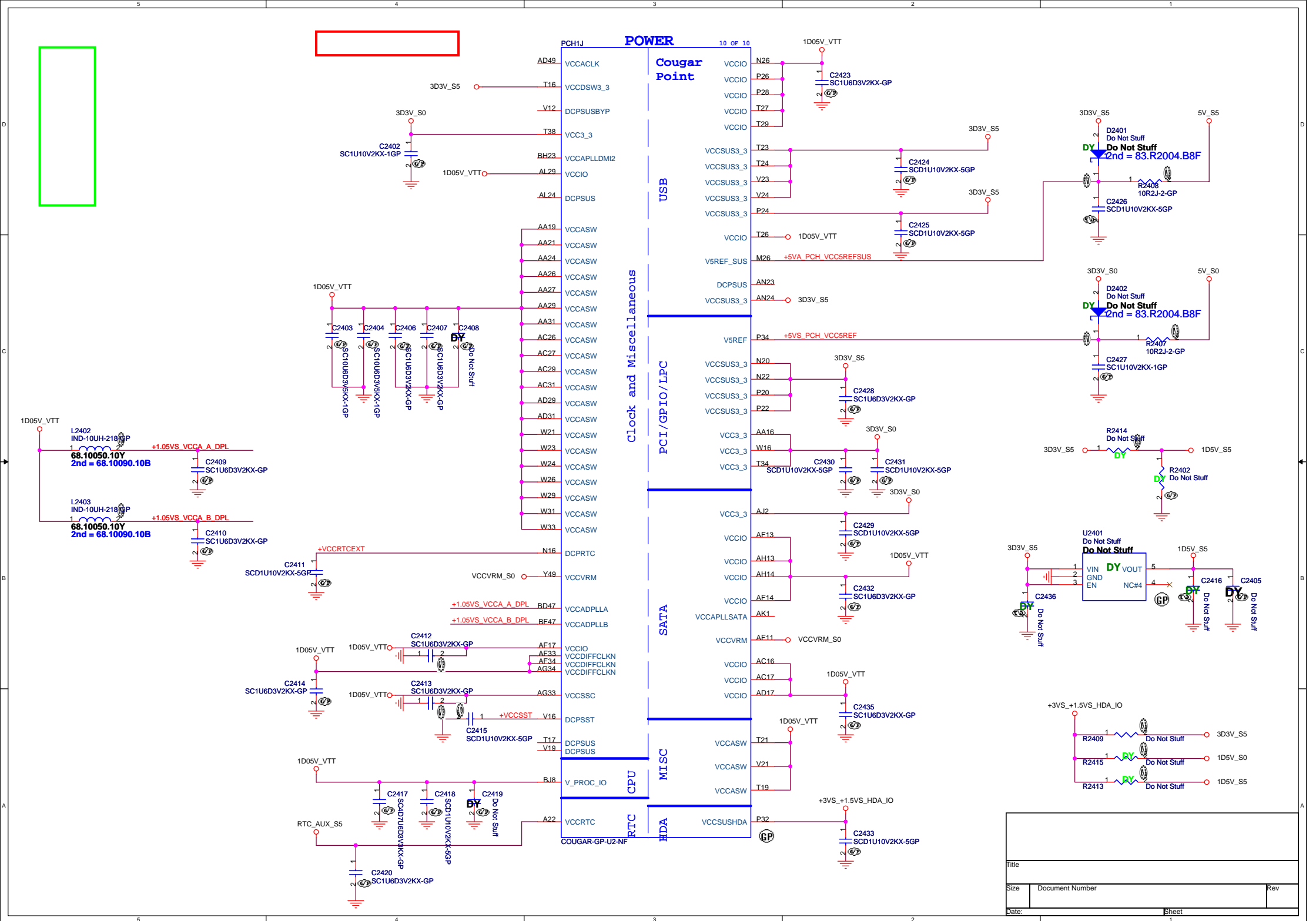


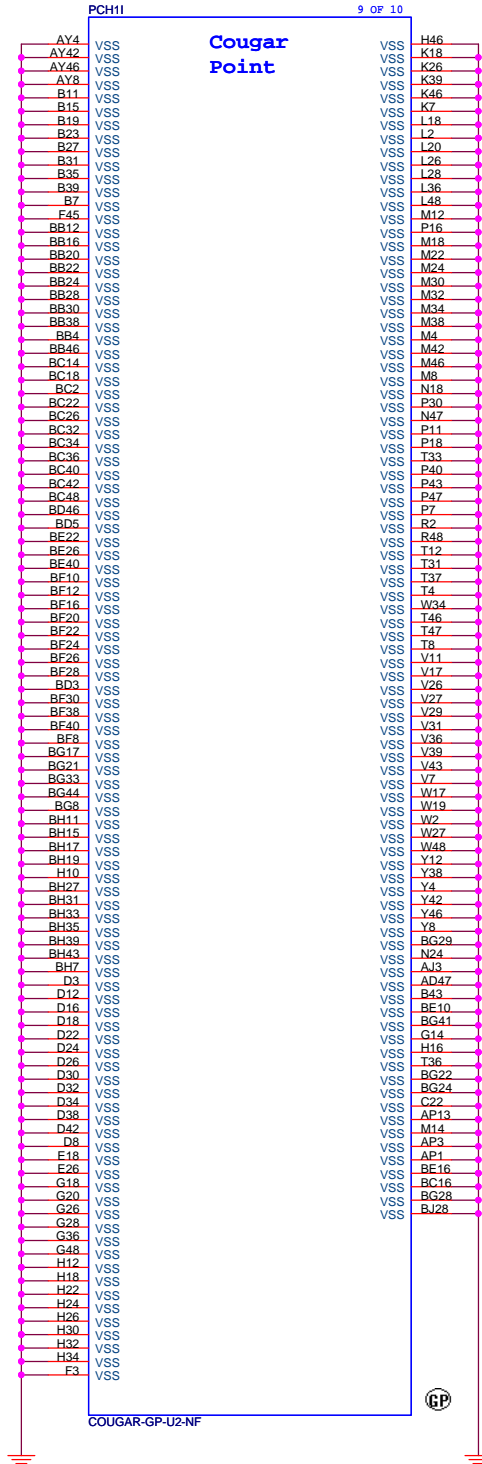
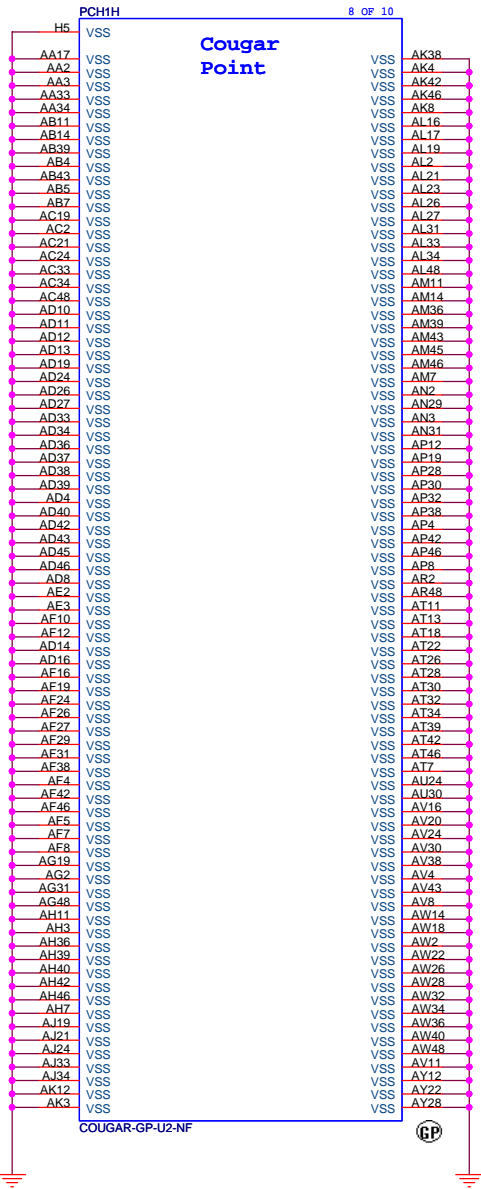
Title		
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Date:	Sheet	

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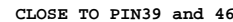
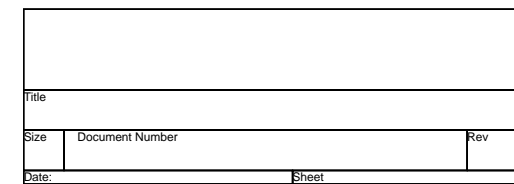
Title		
Size	Document Number	Rev
Date:	Sheet	

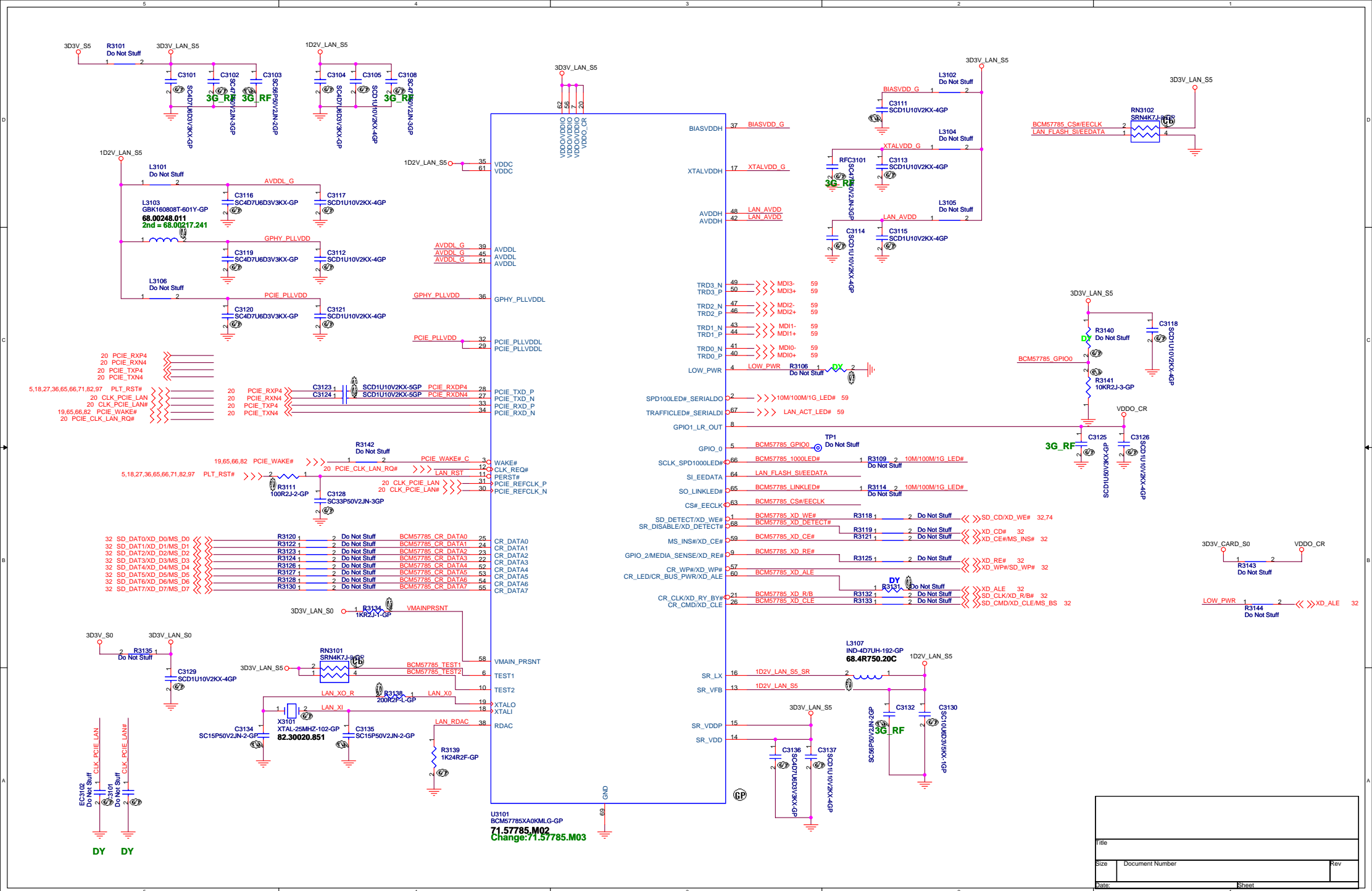




Title		
Size	Document Number	Rev
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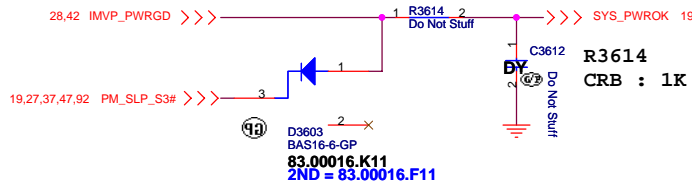


[illegible]

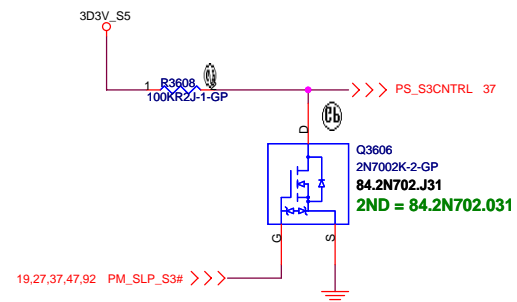
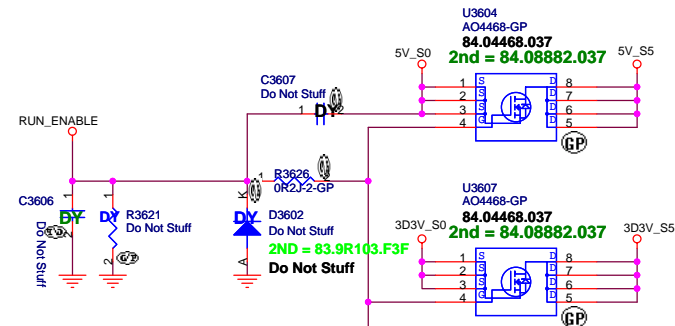
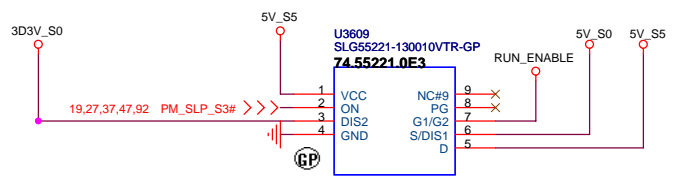


Title		
Size	Document Number	Rev
Date:	Sheet	

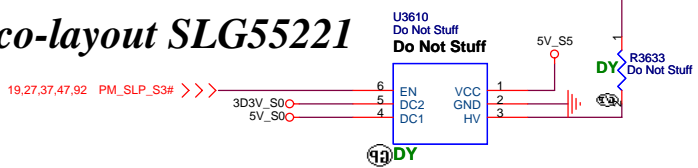
Power Sequence



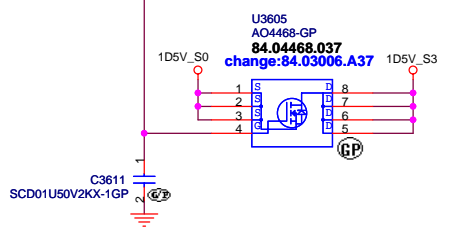
ANNIE Run Power



-1 co-layout SLG55221



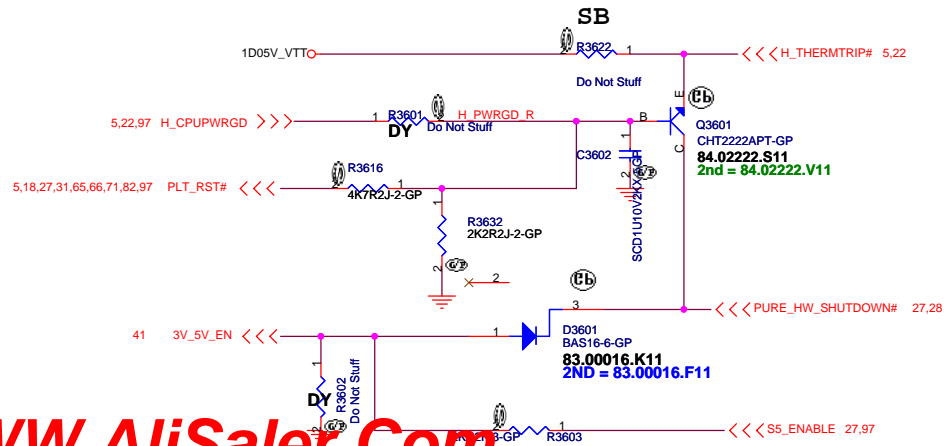
-1 modify R3621,D3602 to DY



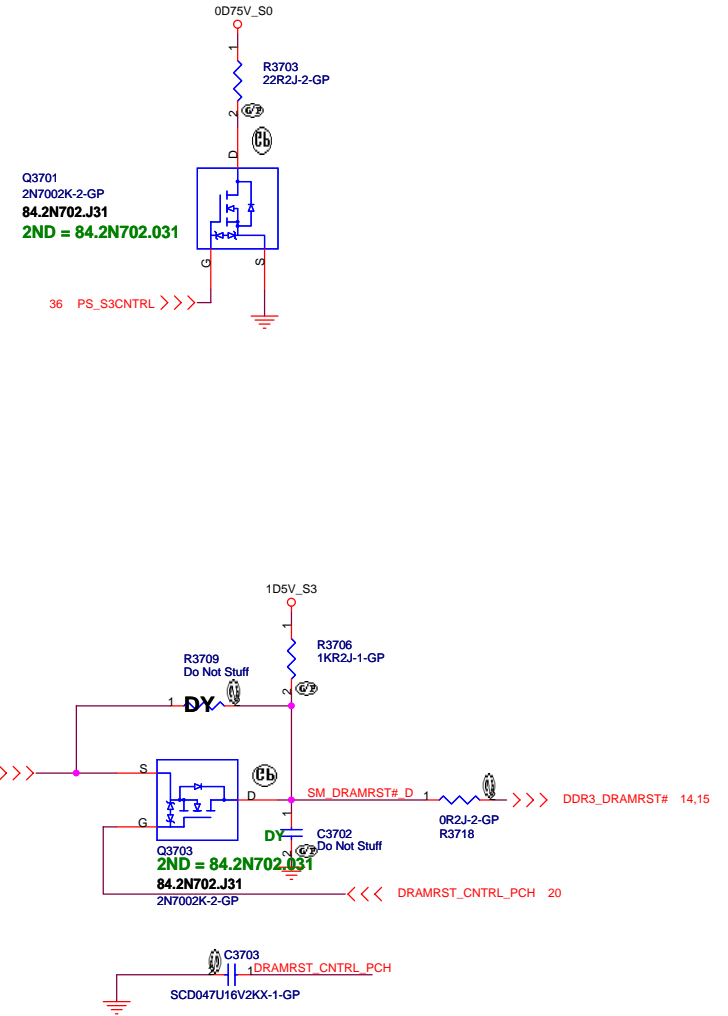
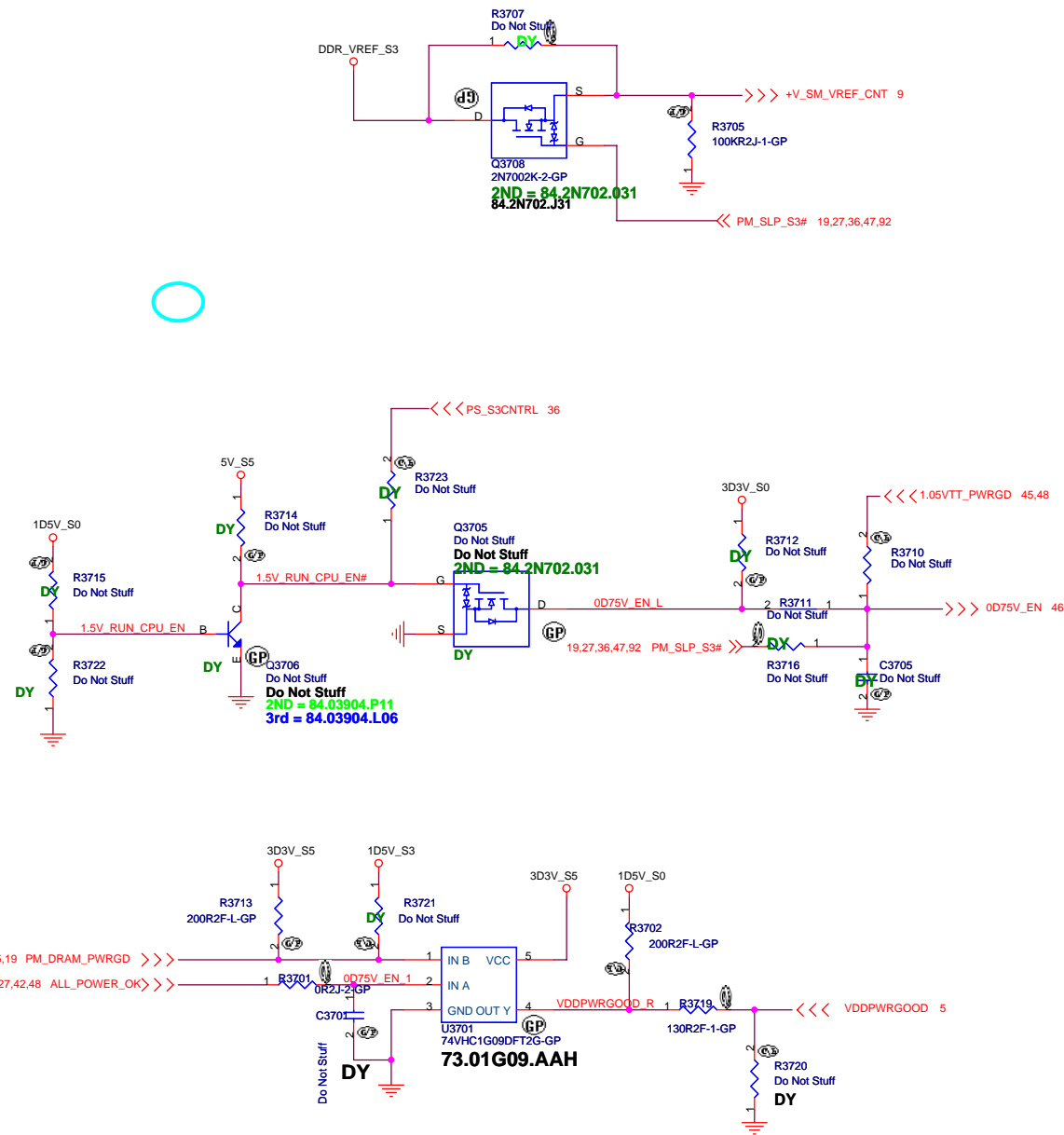
SB modify part number

1D5V_S0

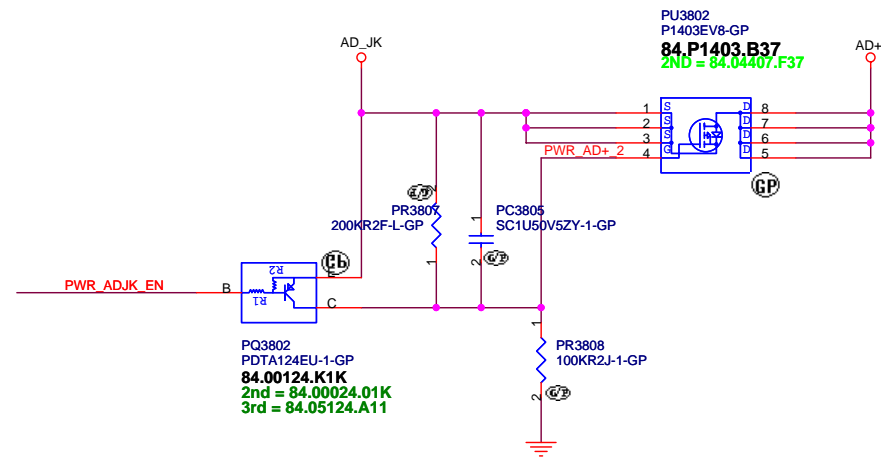
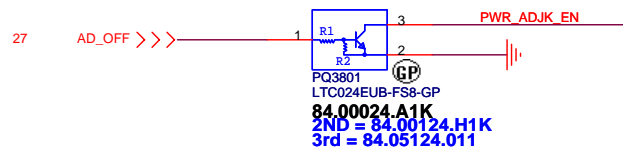
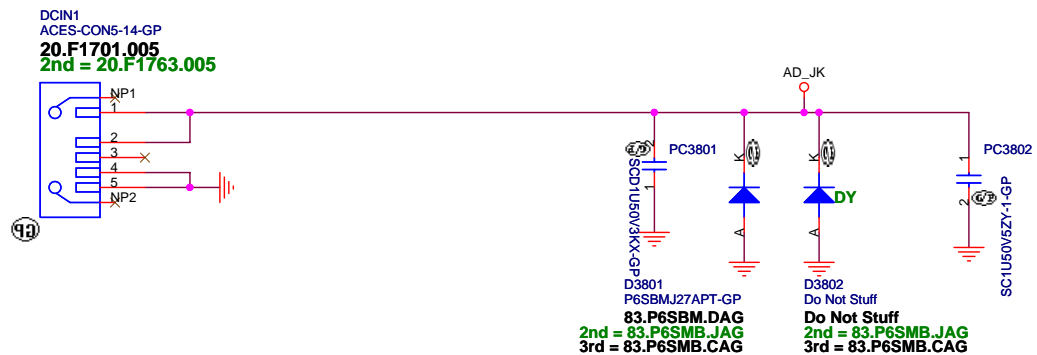
MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A



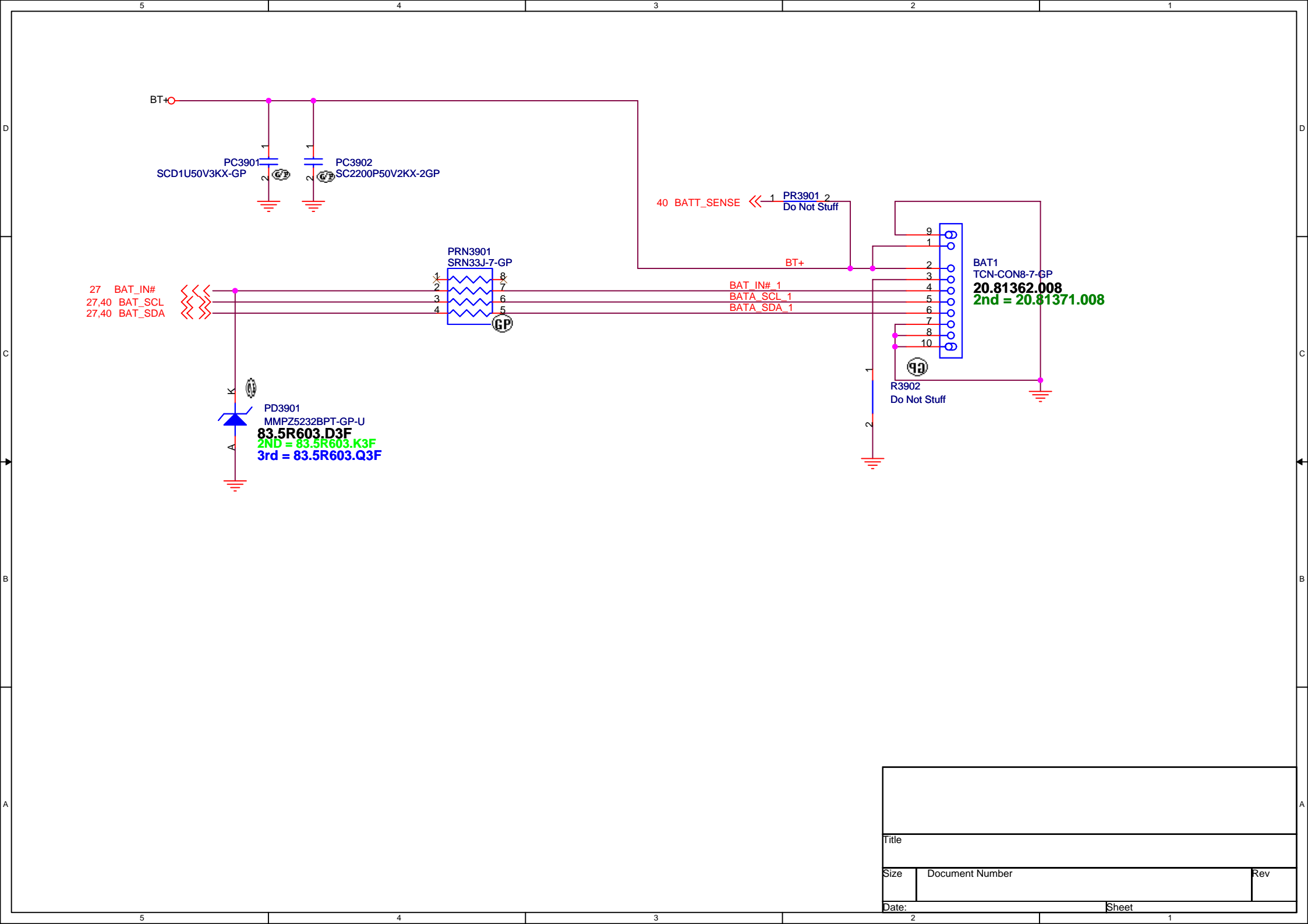
Title		
Size	Document Number	Rev
Date:	Sheet	



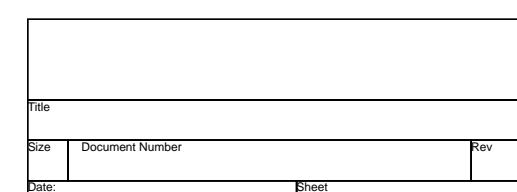
Title		
Size	Document Number	Rev
Date:	Sheet	

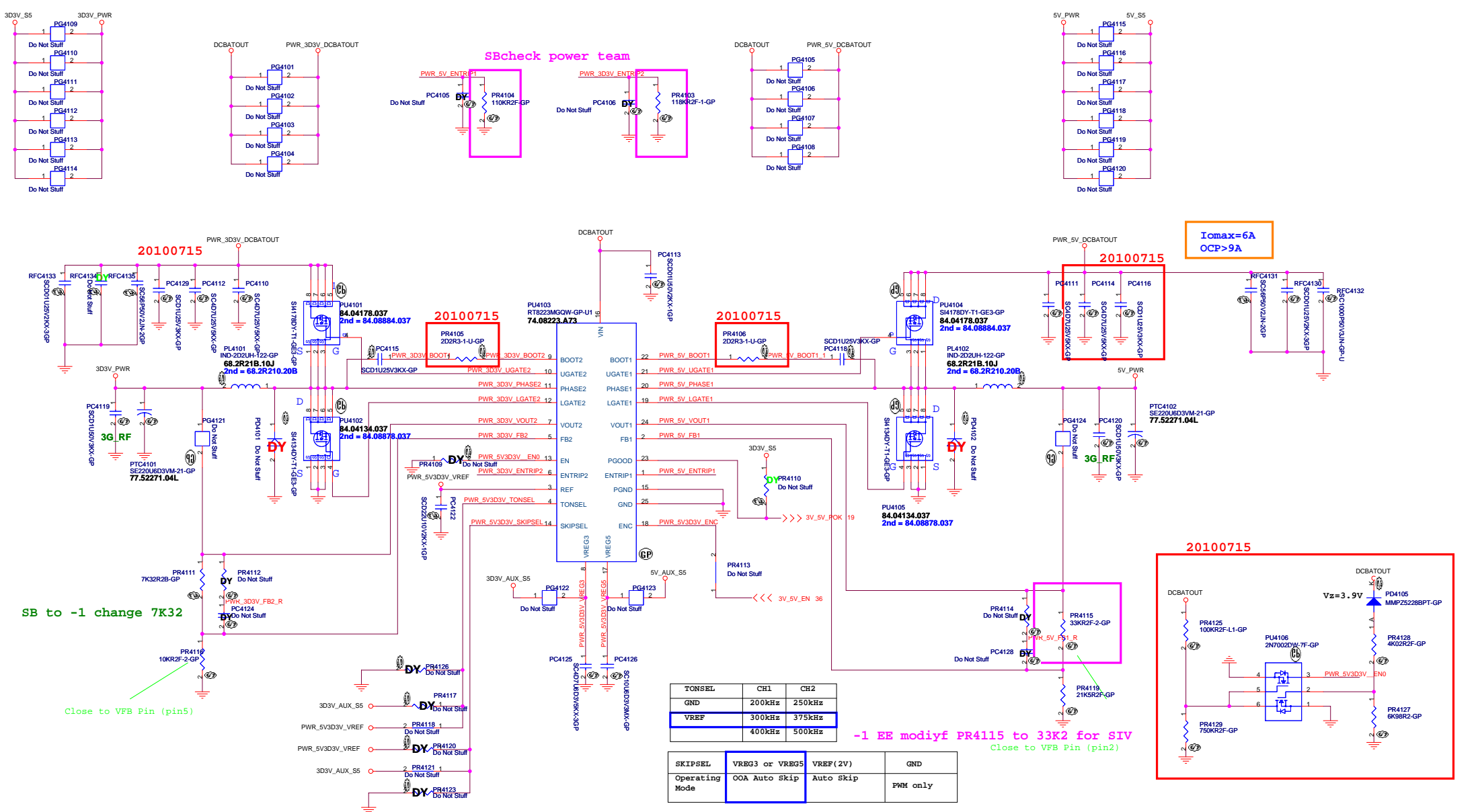


Title		
Size	Document Number	Rev
Date:	Sheet	



Title		
Size	Document Number	Rev
Date: Sheet		

AD+ TO SYS PR4004

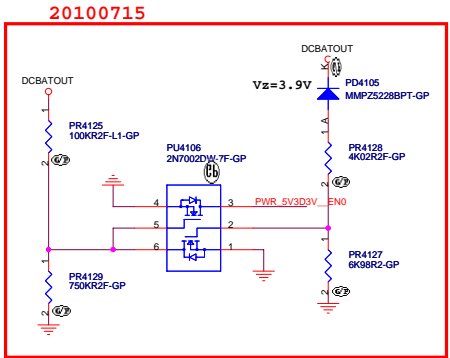


I_{omax}=6A
OCP>9A

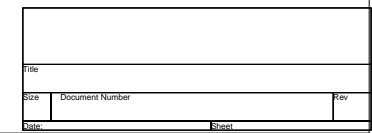
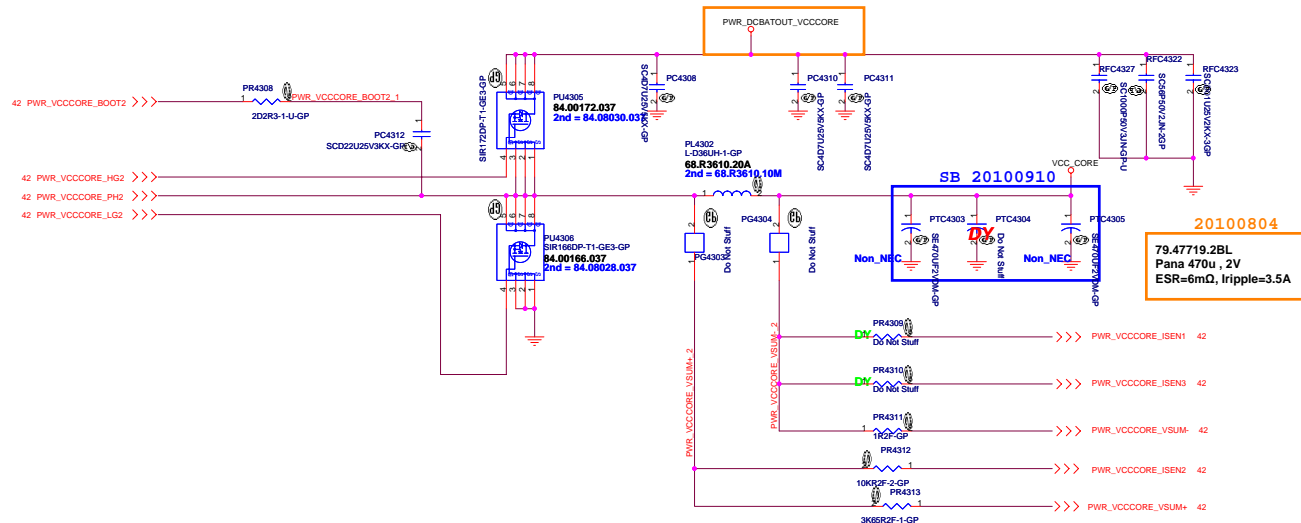
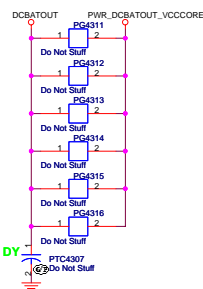
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto skip	Auto skip	PWM only

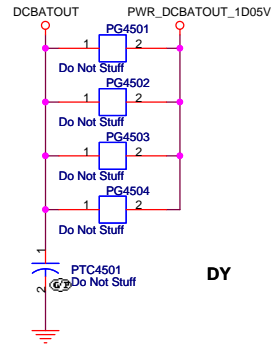
-1 EE modiyf PR4115 to 33K2 for SIV
Close to VFB Pin (pin2)



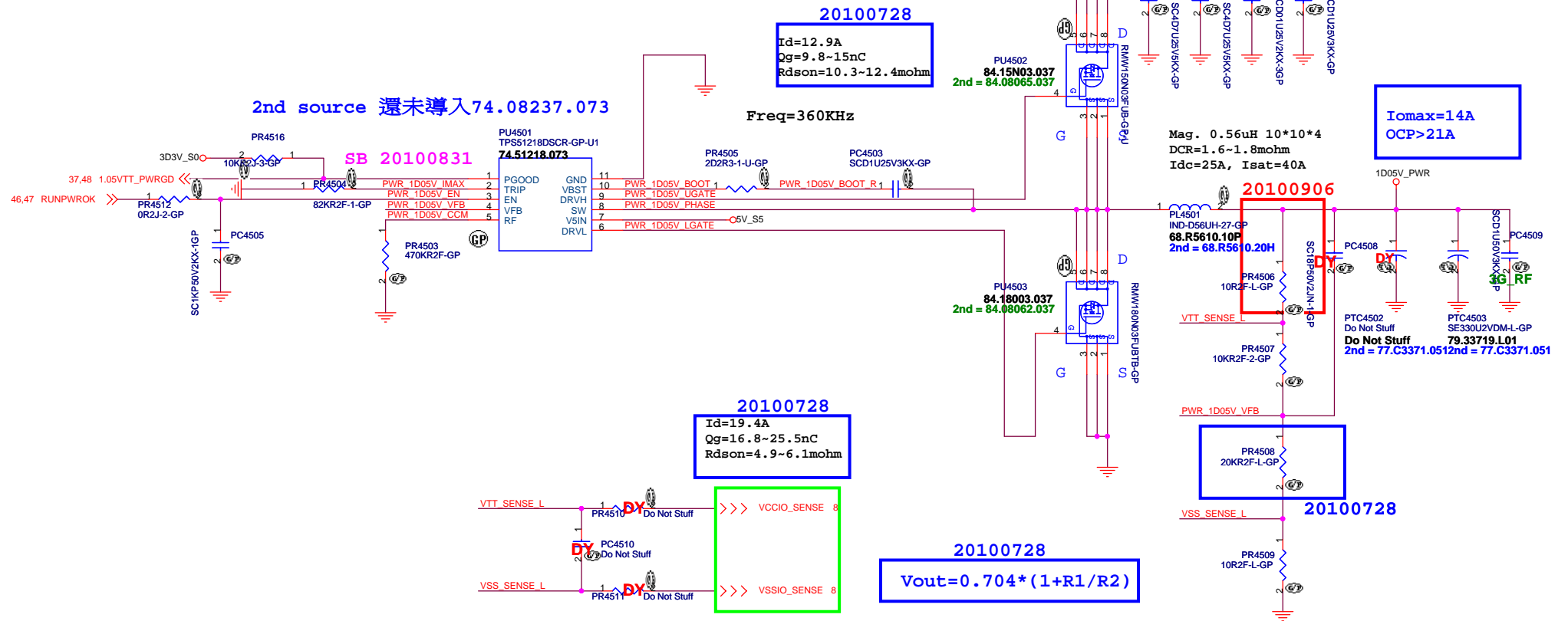
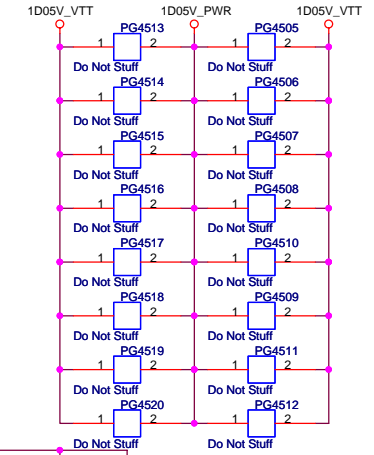
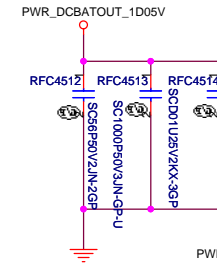
File		
Size	Document Number	Rev
Date		Sheet



TPS51218D for 1D05V

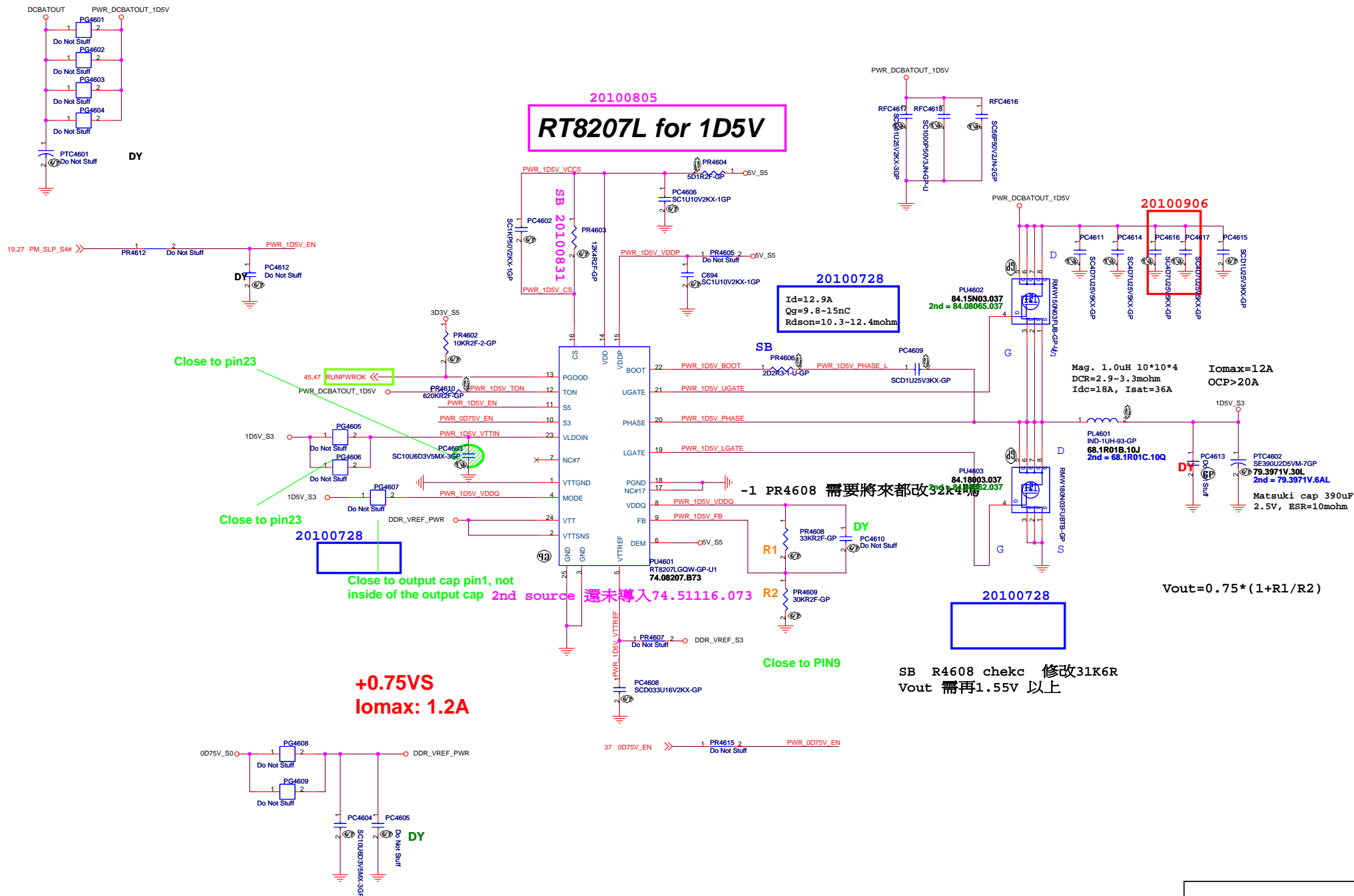


DY



Title		
Size	Document Number	Rev
Date:	Sheet	

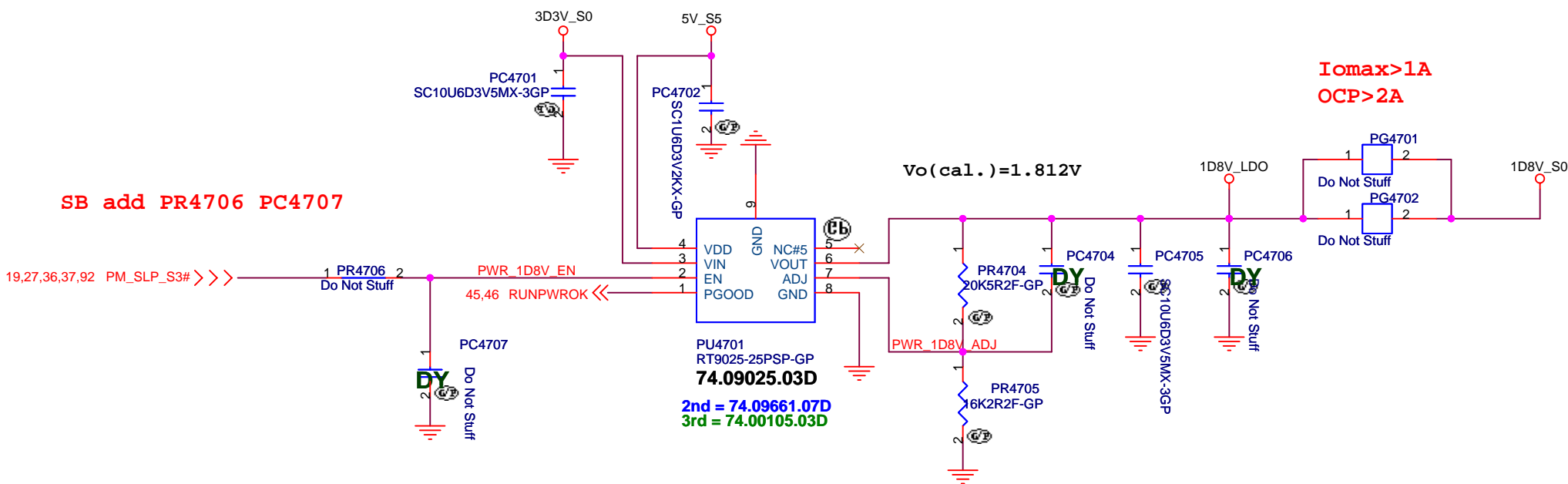
```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



Title		
Size	Document Number	Rev
Date:	Sheet	
1		

SSID = PWR.Plane.Regulator_1p8v

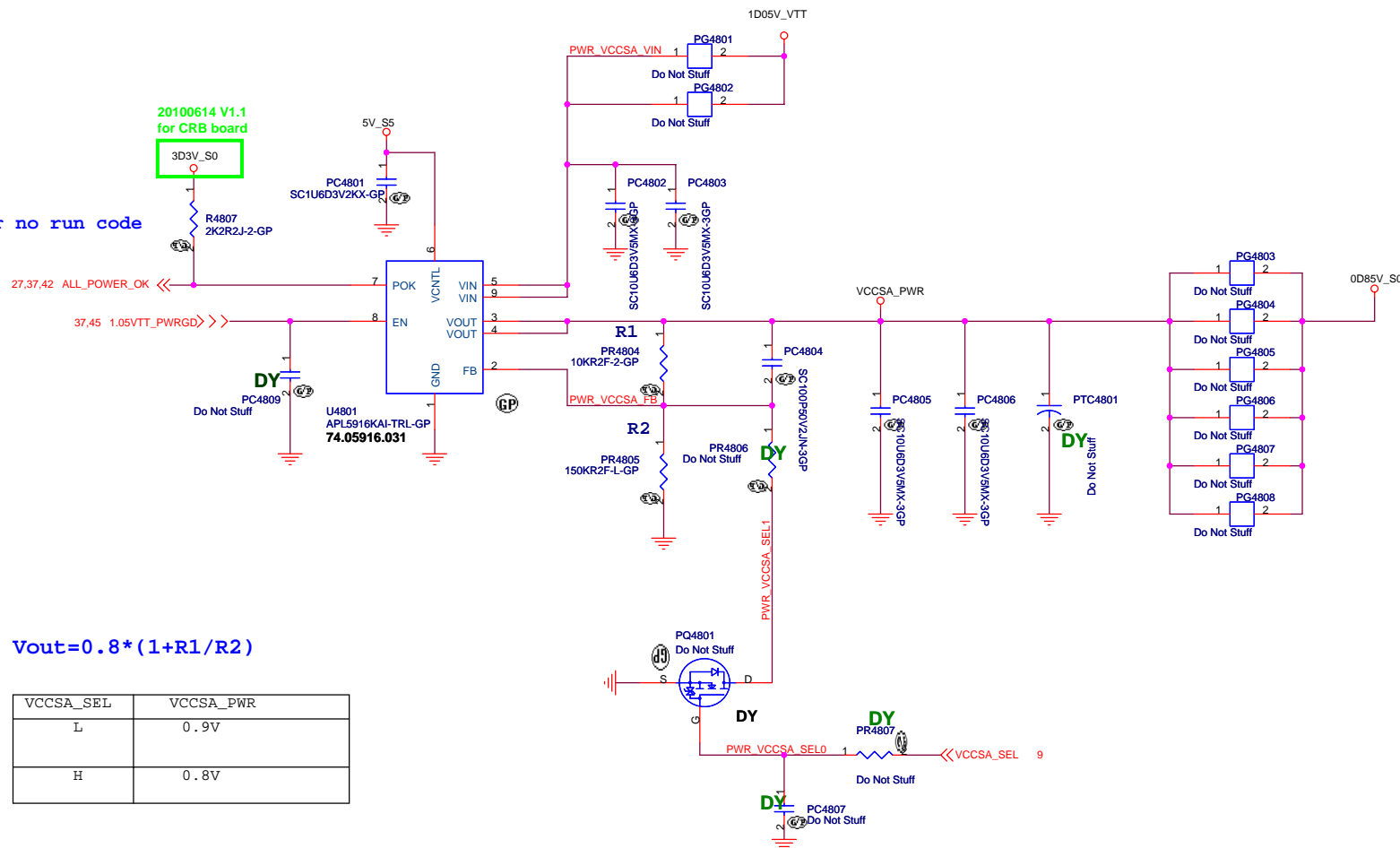
RT9025 for 1D8V_S0



Title		
Size	Document Number	Rev
Date:		Sheet

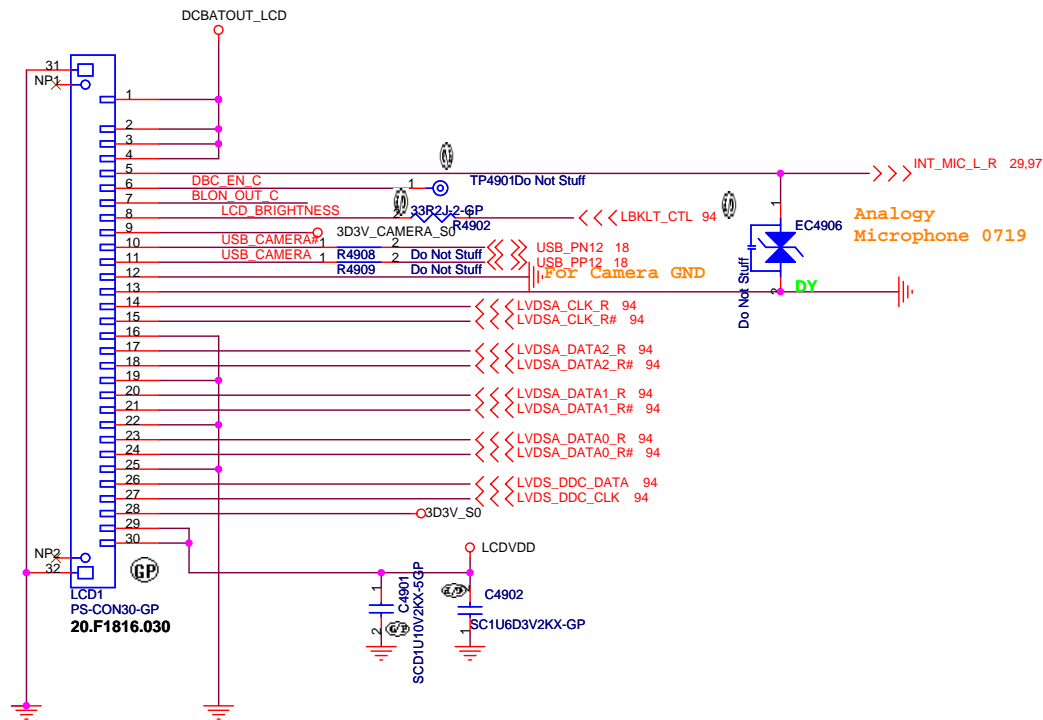
APL5916 for VCCSA

SB modify 2K2 for no run code

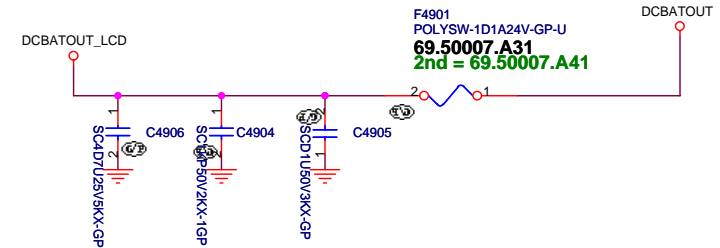


Title		
Size	Document Number	Rev
Date:	Sheet	

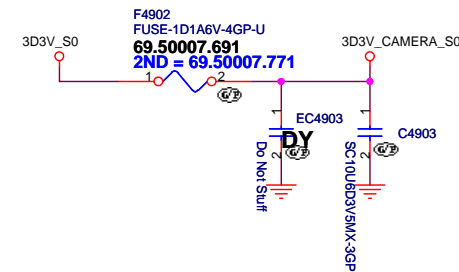
LVDS CONNECTOR



INVERTER POWER

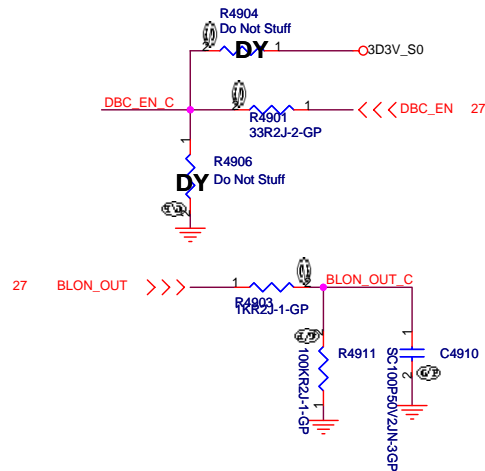
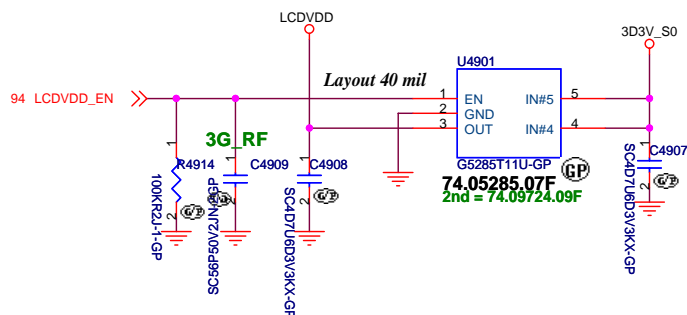


Camera Power

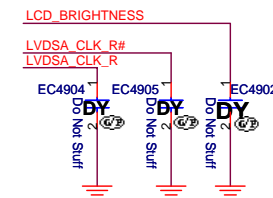


SSID = VIDEO

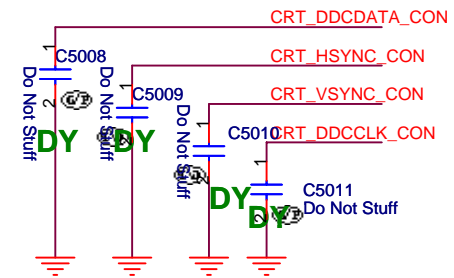
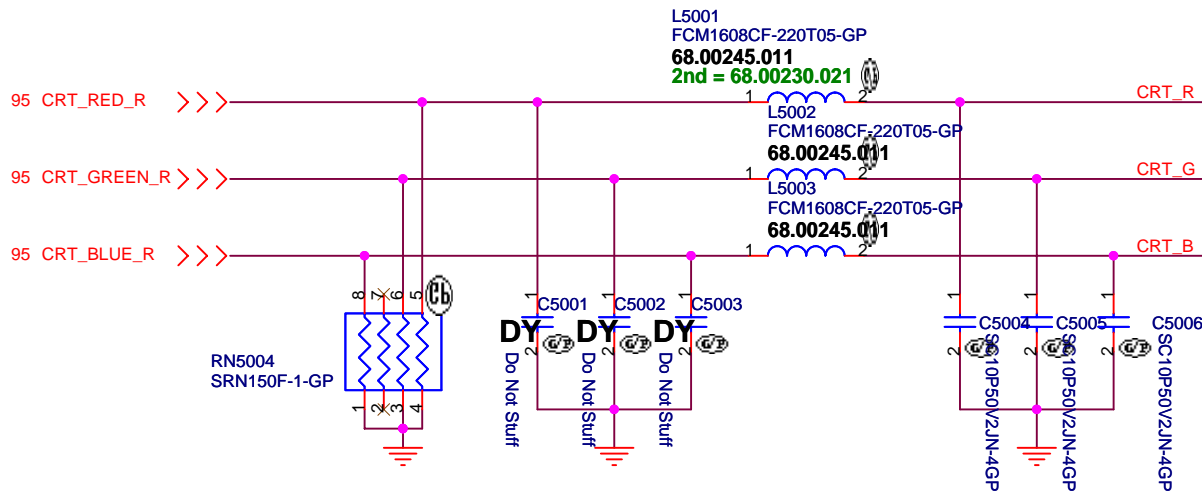
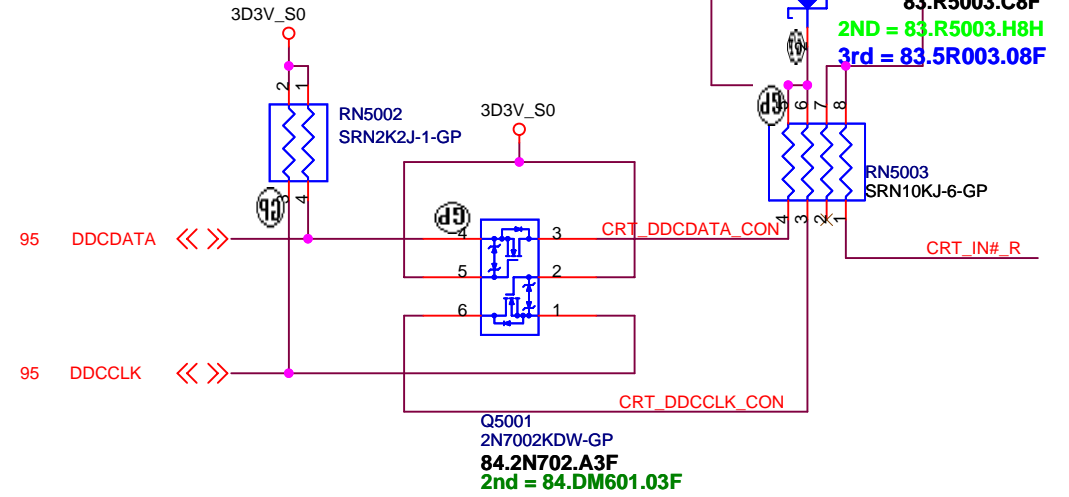
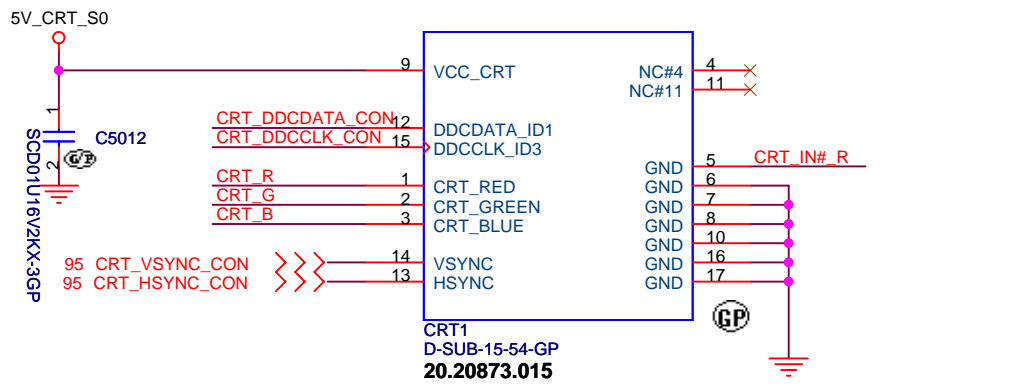
LCD POWER for ANNIE



For EMI request
Close to LVDS connector



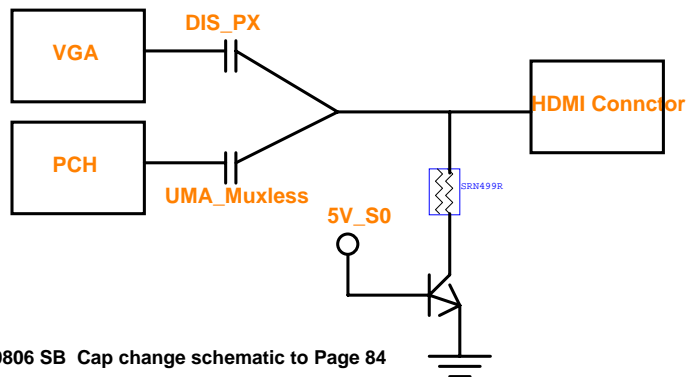
Title		
Size	Document Number	Rev
Date:	Sheet	



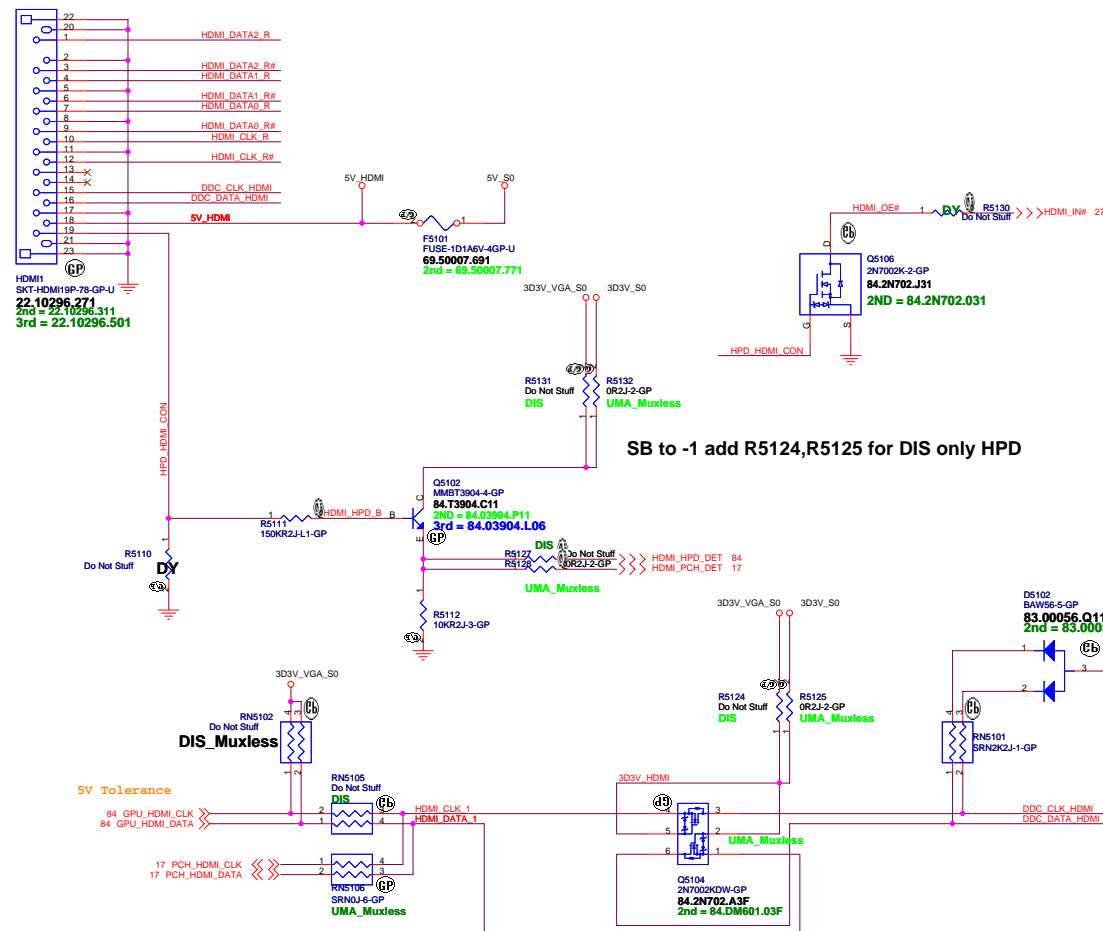
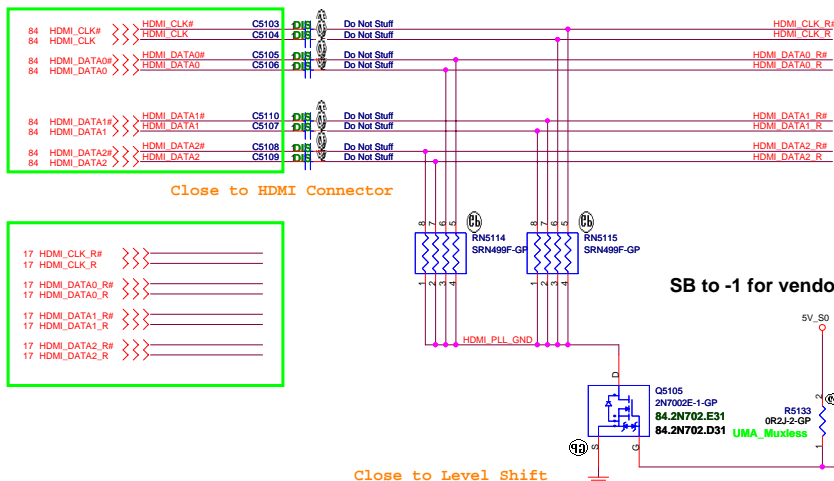
Title		
Size	Document Number	Rev
Date:	Sheet	

HDMI CONN

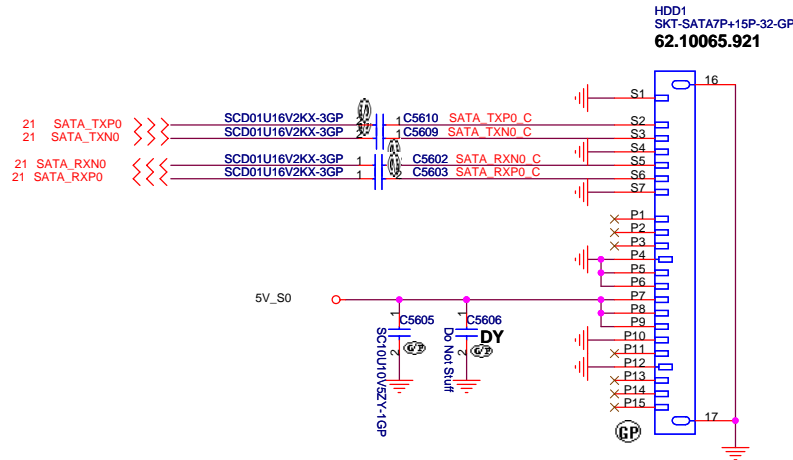
HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84

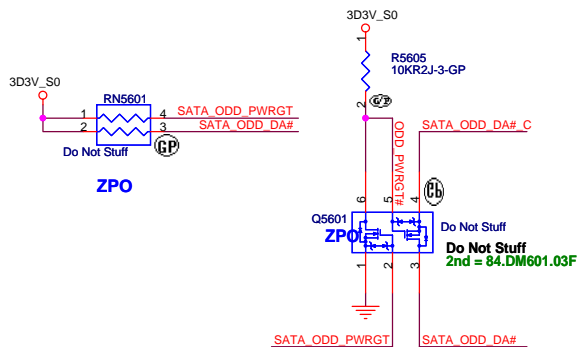
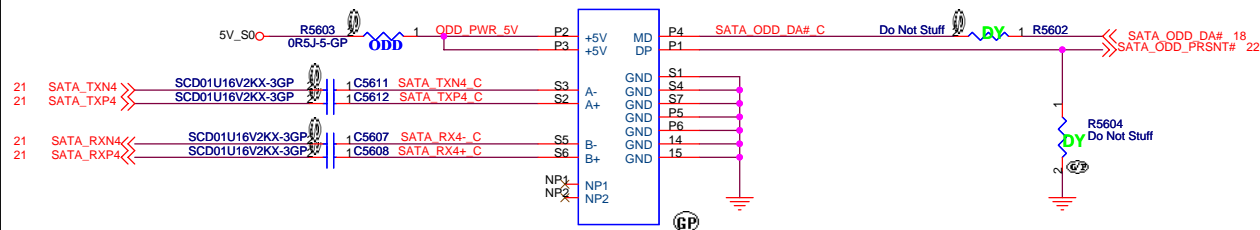


Title		
Size	Document Number	Rev
Date:	Sheet	



ODD Connector

ODD1
SKT-SATA7P-6P-90-GP
22.10300.C11

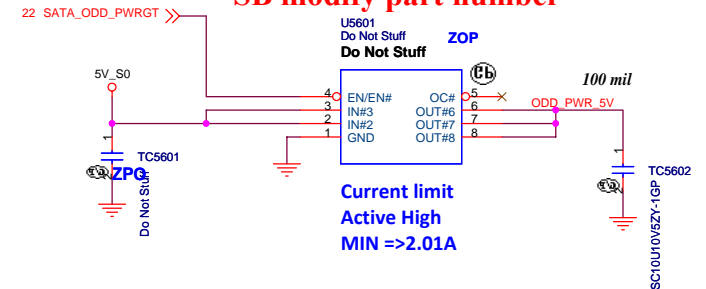


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



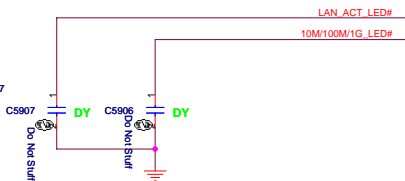
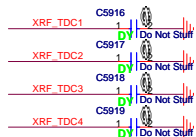
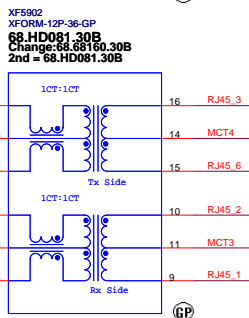
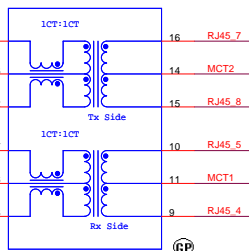
Title		
Size	Document Number	Rev
Date:	Sheet	

GIGA Lan Transformer

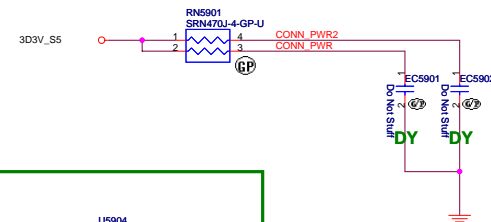
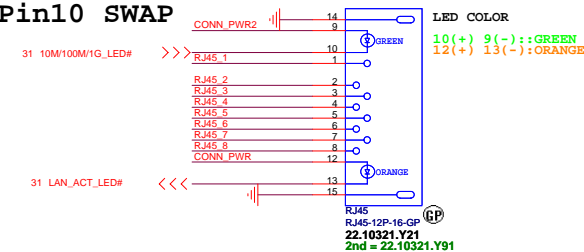


LAN MDI Off-Page

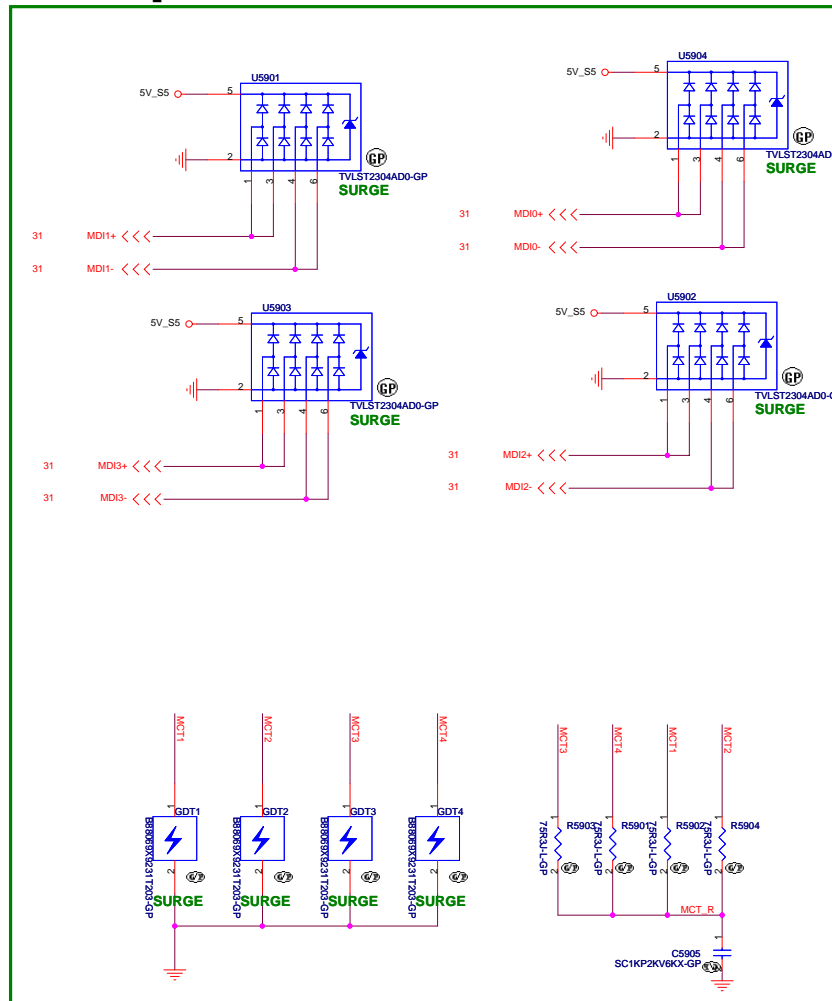
XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B



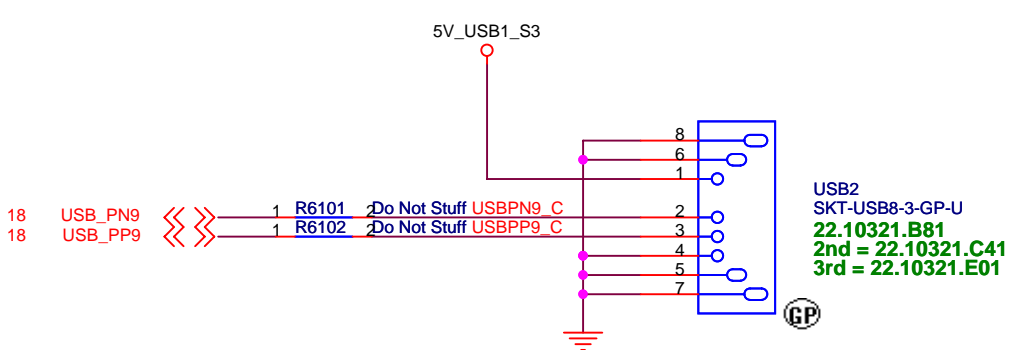
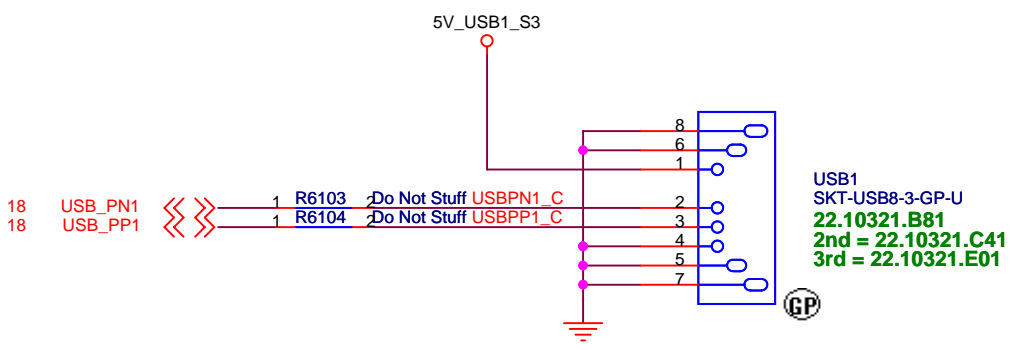
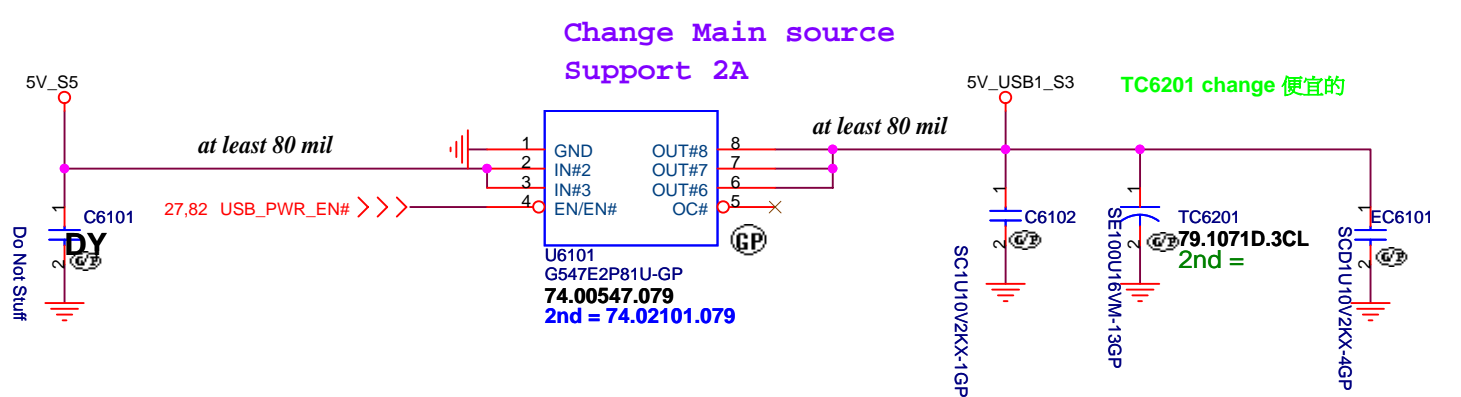
SB modiyf Pin9 Pin10 SWAP



SB modify For EMI



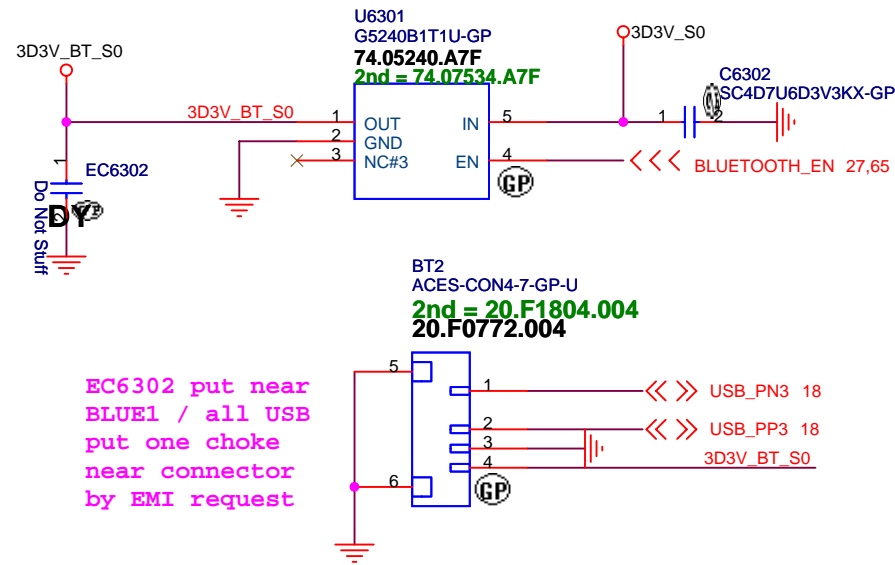
Title	Document Number	Rev
Date:	Sheet	



Title		
Size	Document Number	Rev
Date:		Sheet

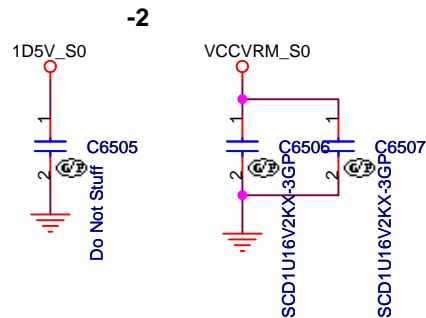
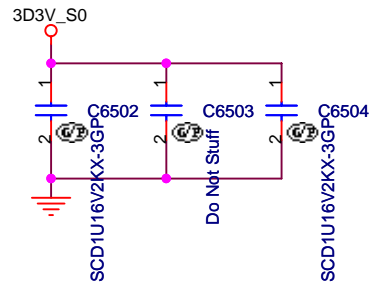
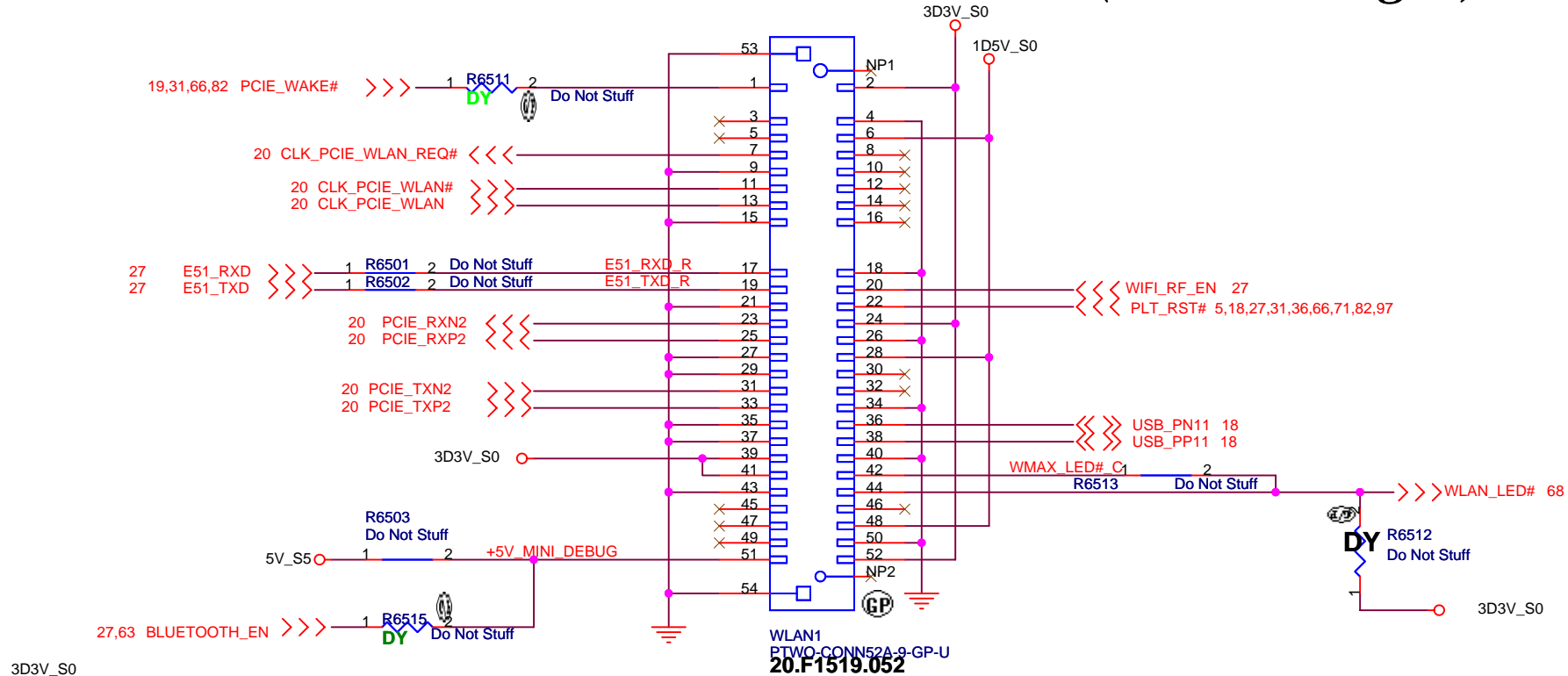
Bluetooth Module conn.

ANNIE Bluetooth Module

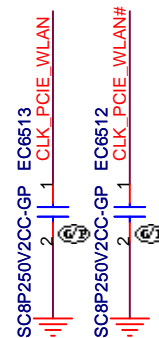


Title		
Size	Document Number	Rev
Date:		Sheet

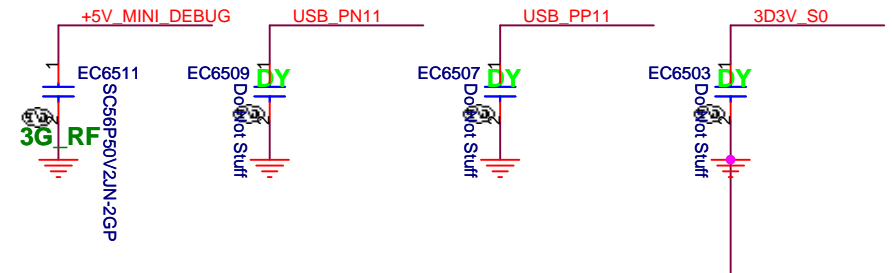
Mini Card Connector(802.11a/b/g/n)



SB modify for SIV



RF suggestion

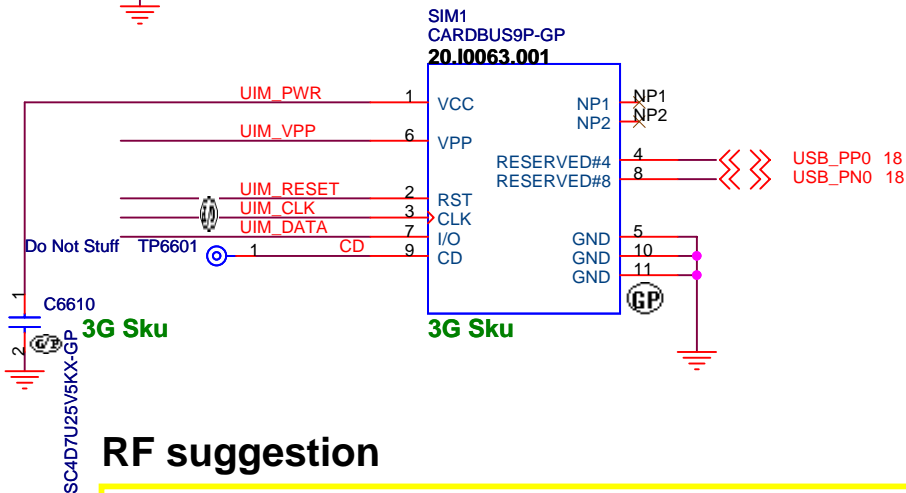
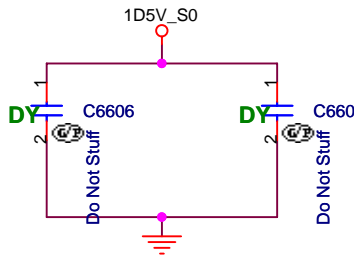
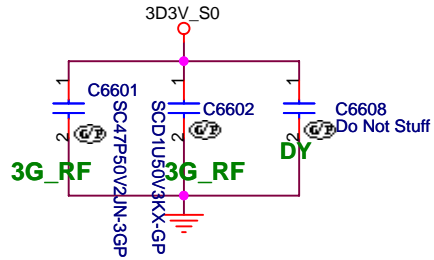


Title		
Size	Document Number	Rev
Date		Sheet

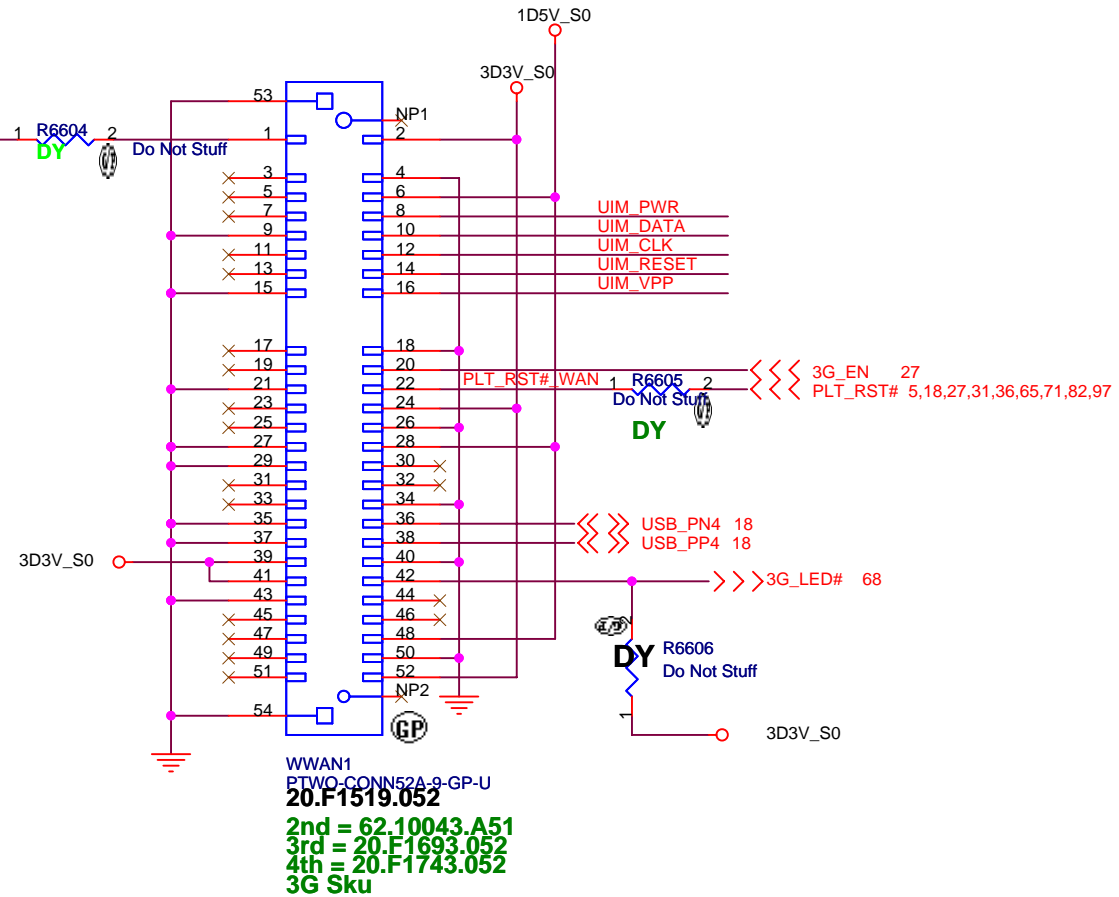
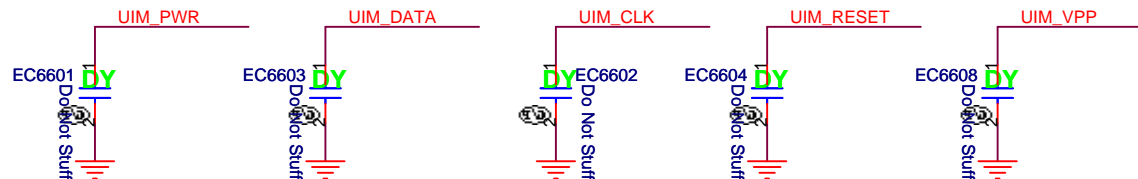
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN

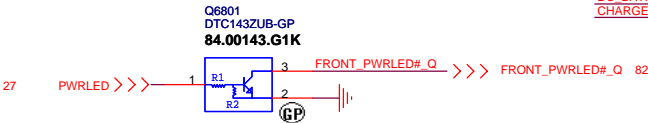


RF suggestion

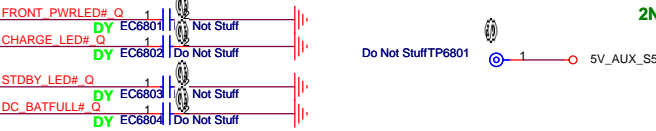
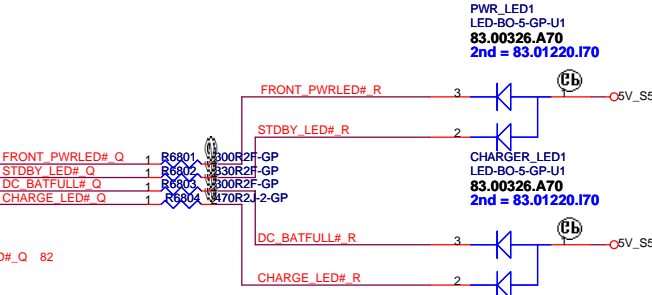
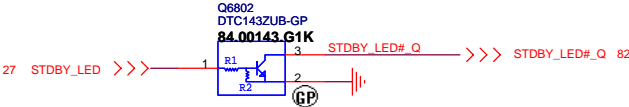


Title		
Size	Document Number	Rev
Date:	Sheet	

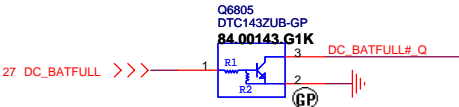
Power button LED



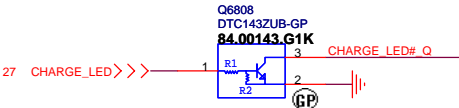
Power STDBY_LED



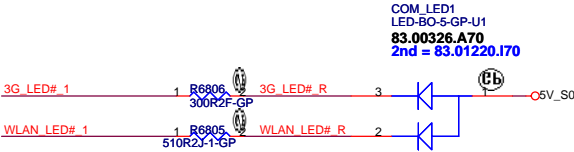
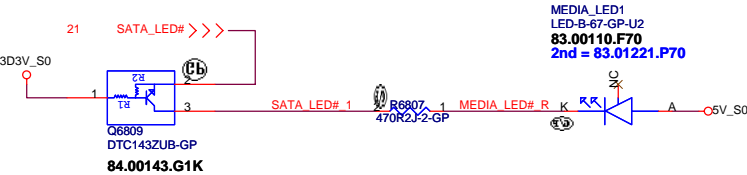
Battery LED2(DC_BATFULL)



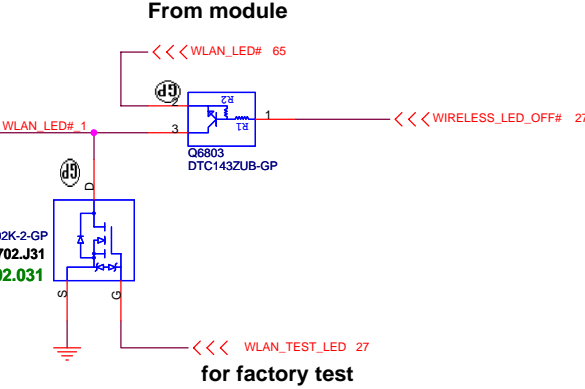
Battery LED1(CHARGE)



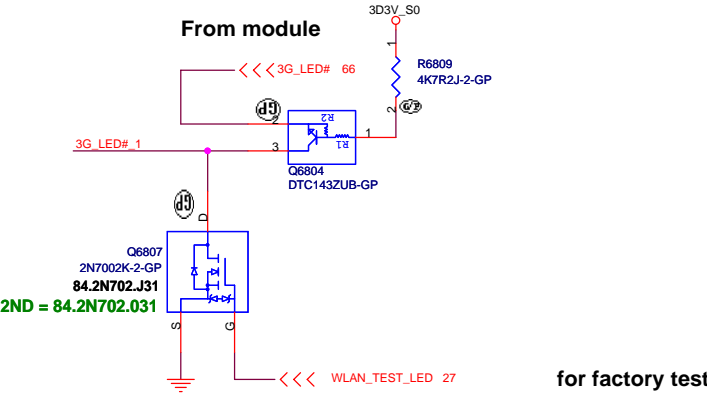
SATA HDD LED



WLAN_LED

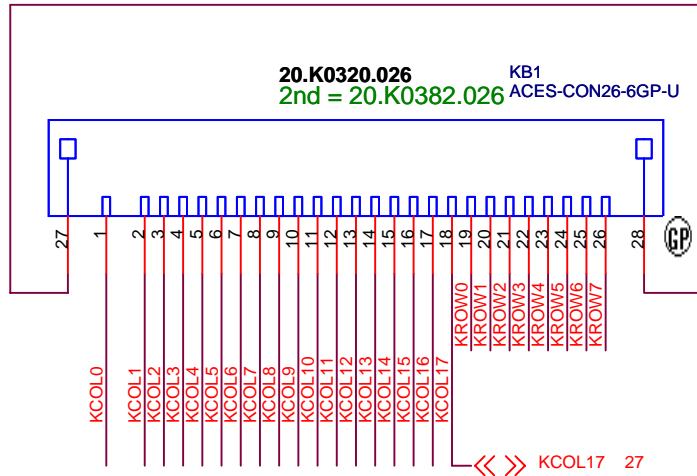


3G LED



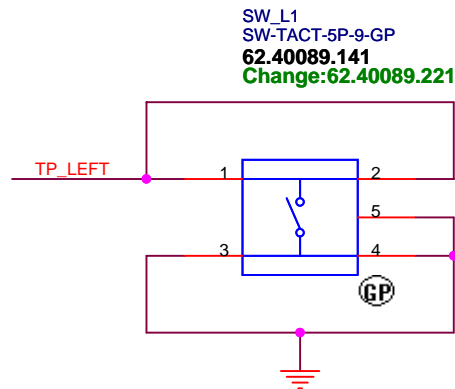
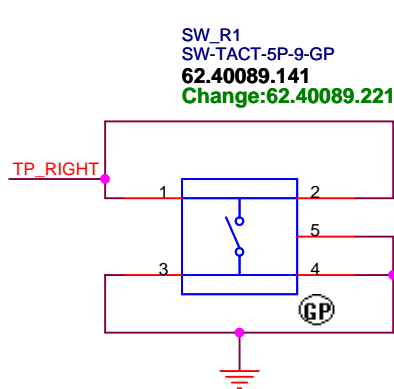
Title		
Size	Document Number	Rev
Date:	Sheet	

Internal KeyBoard Connector

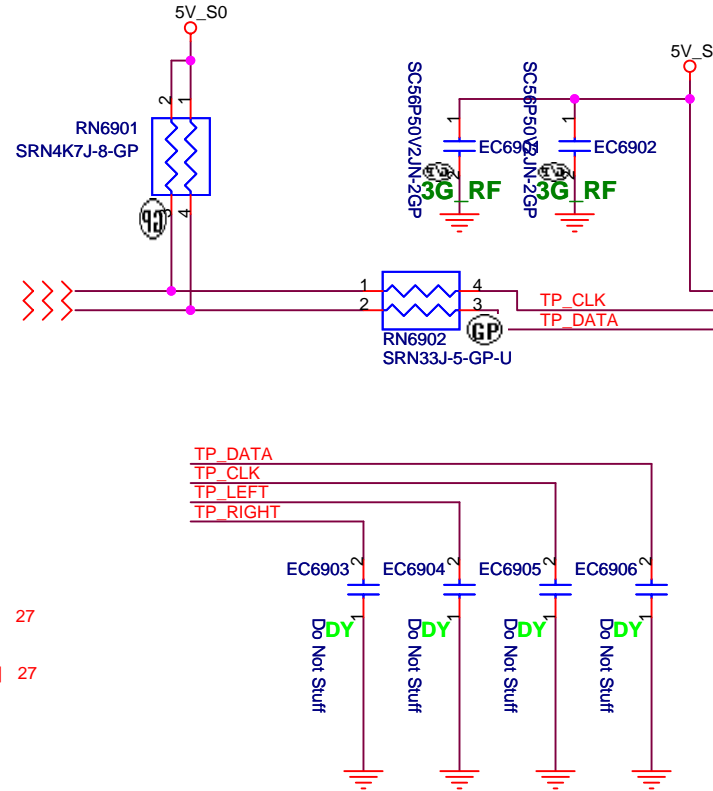


MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

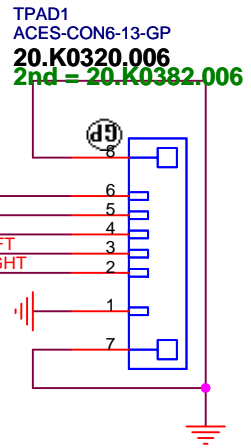
26 **K/B** 1 **SB to -1 modify Part number**



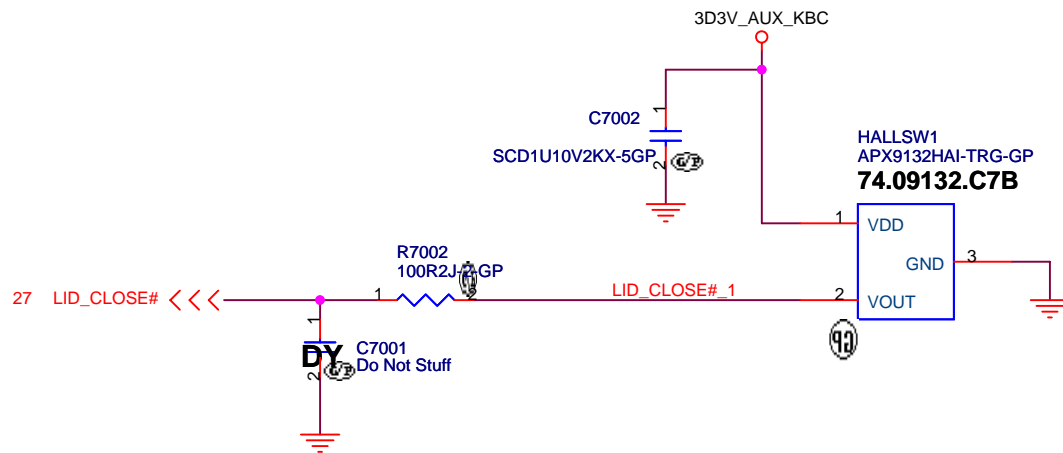
TOUCH PAD



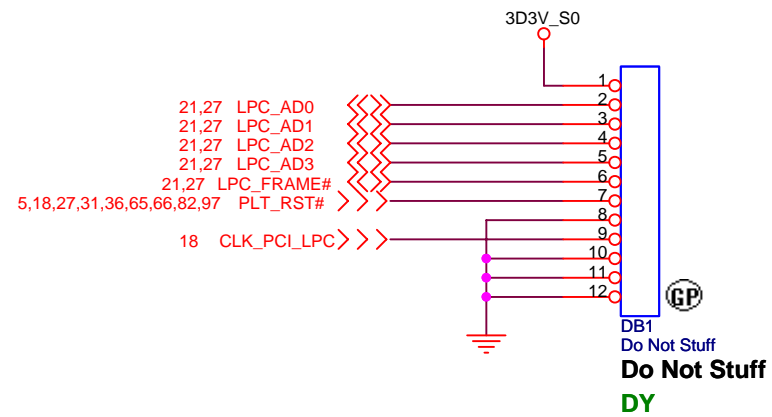
FFC 異面



Title		
Size	Document Number	Rev
Date:	Sheet	

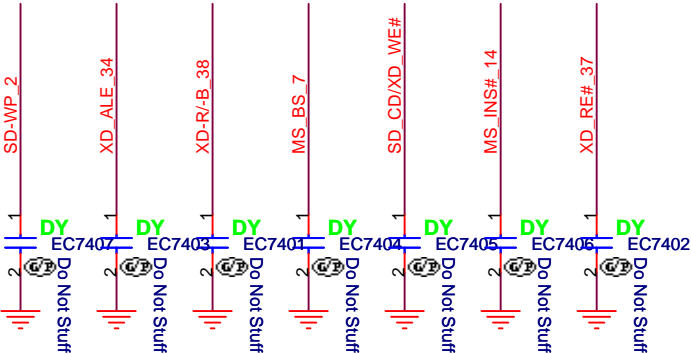
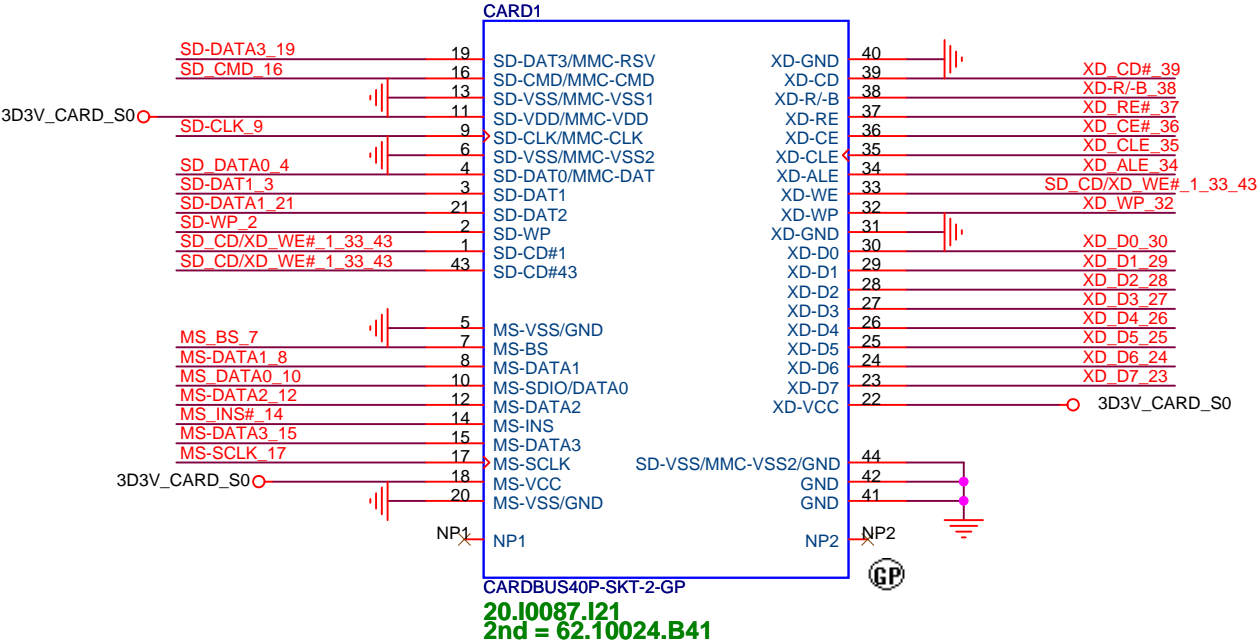
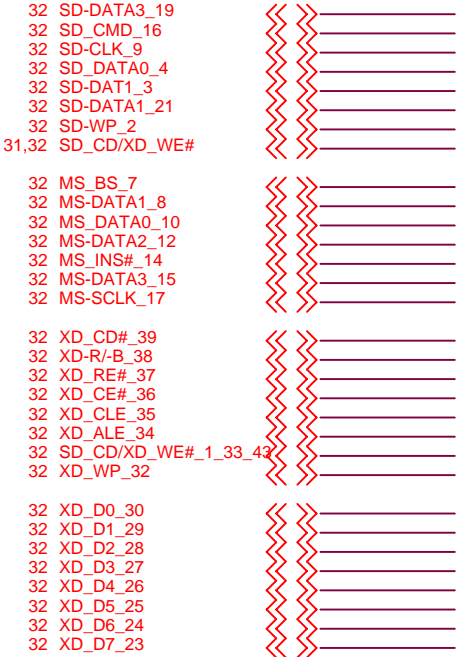


Title		
Size	Document Number	Rev
Date:		Sheet

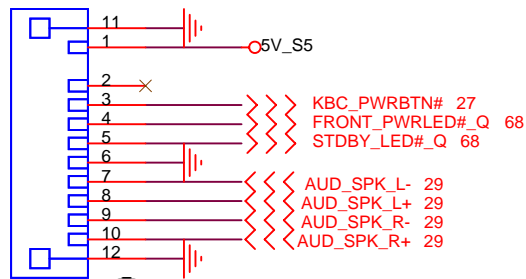


Title		
Size	Document Number	Rev
Date:		Sheet

SD/XD/MS Card Reader



Title		
Size	Document Number	Rev
Date	Sheet	



PWRN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010

R8105
Do Not Stuff

AUD_AGND

1D5V_S3

29 EXT_MIC_JD#
29 MIC_IN_R
29 MIC_IN_L

19,31,65,66 PCIE_WAKE#
18 USB30_SMI#

29 COMBO_MIC
29 AUD_HP1_JACK_R2
29 AUD_HP1_JD#
29 AUD_HP1_JACK_L2

18 USB_PN8
18 USB_PP8

27,61 USB_PWR_EN#

5,18,27,31,36,65,66,71,97 PLT_RST

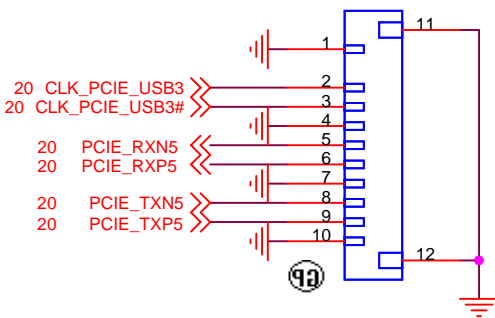
3D3V_S5

20 USB3_PEGB_CLKREQ#

5V_S5

USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026

USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010

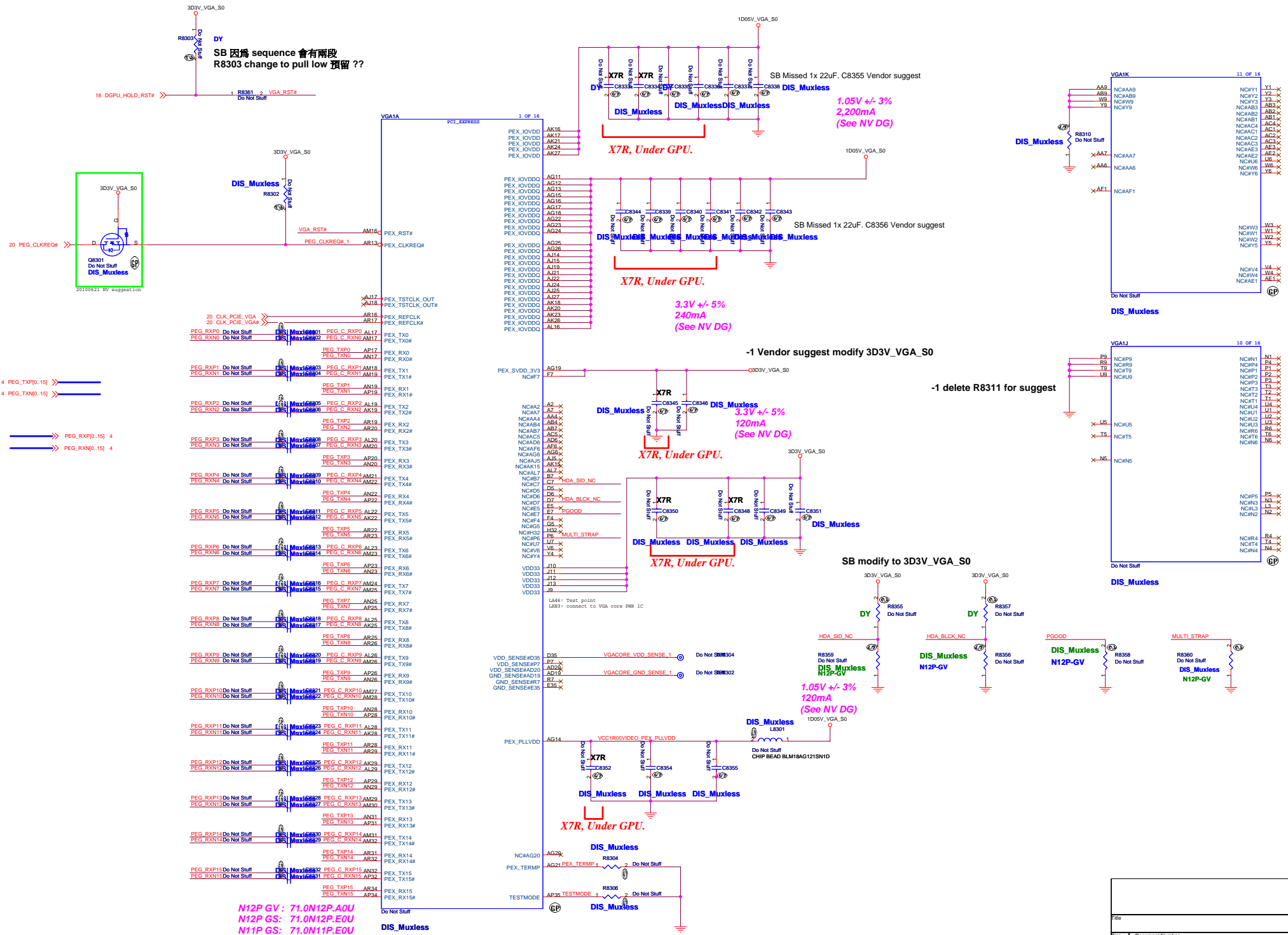


RF_CN1
ACES-CON2-11-GP
20.F0772.002

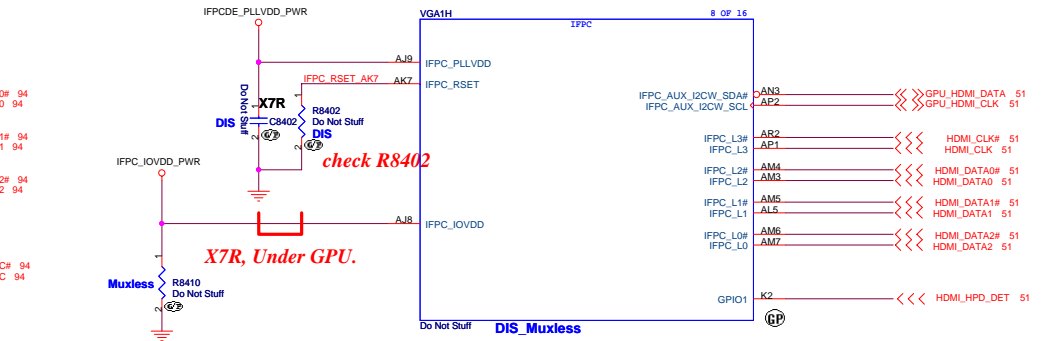
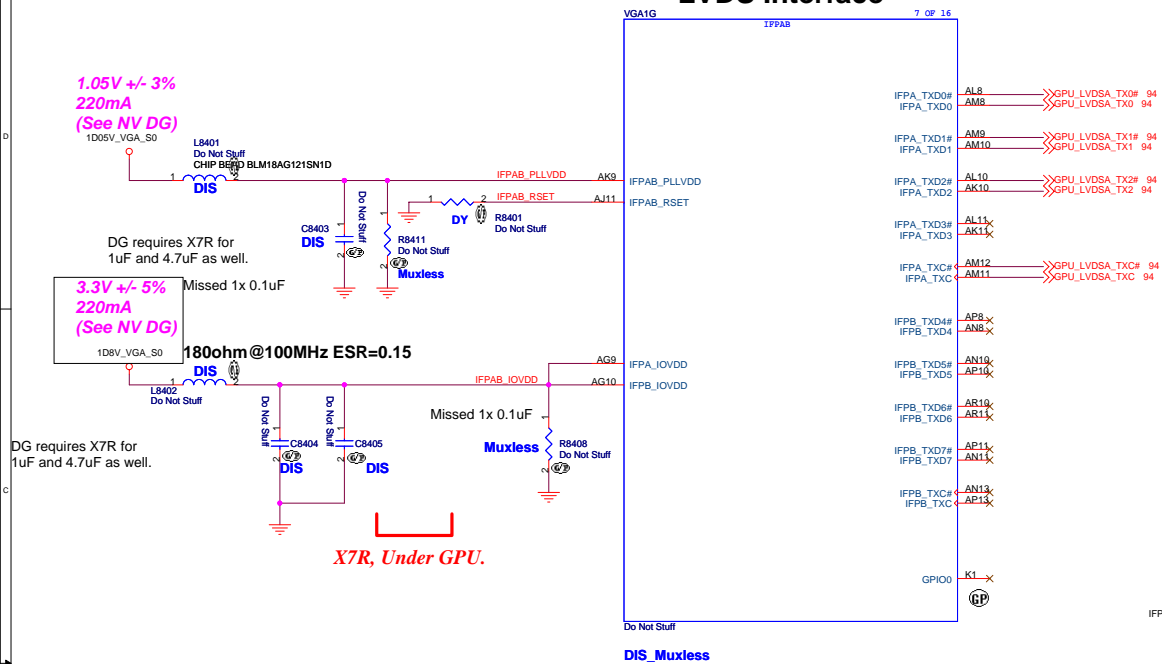
BAE40

27 Wireless_SW

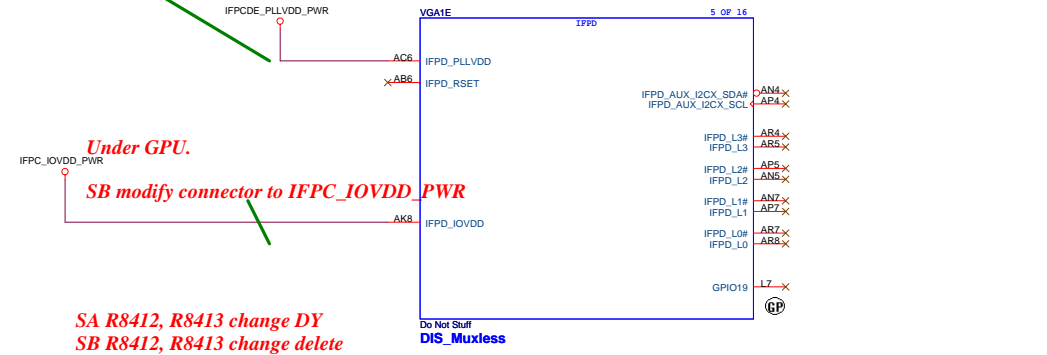
Title		
Size	Document Number	Rev
Date:		Sheet



LVDS Interface



SB modify connector to IFPCDE_PLLVDD_PWR

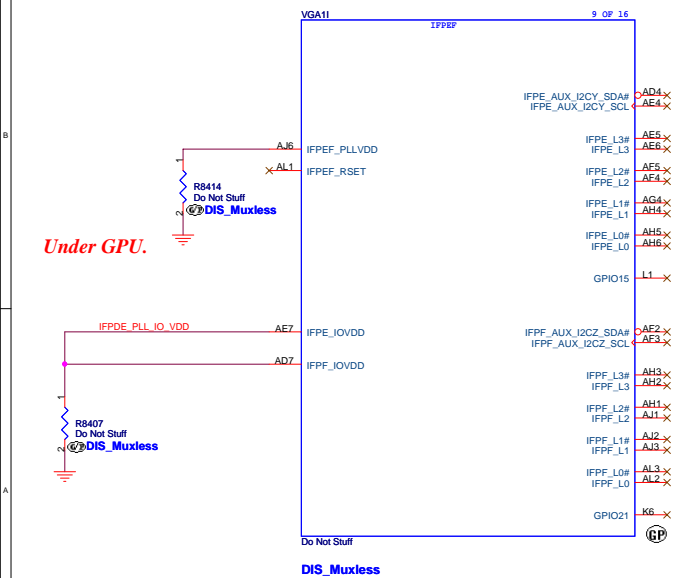


Under GPU.

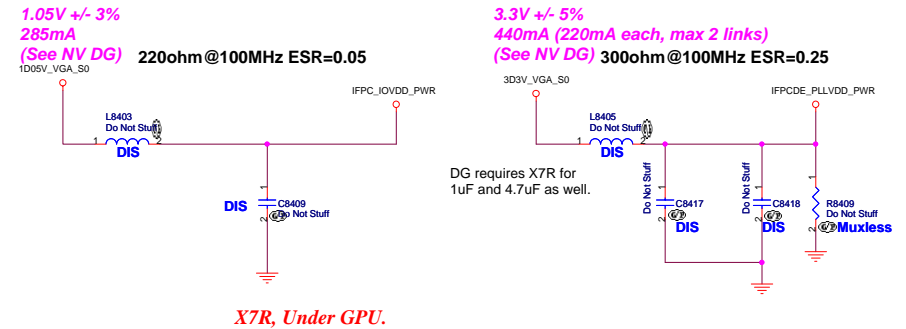
SB modify connector to IFPC_IOVDD_PWR

SA R8412, R8413 change DY
SB R8412, R8413 change delete

HDMI Interface

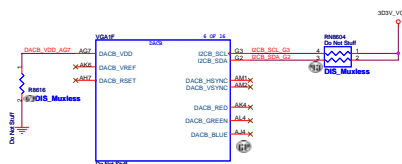
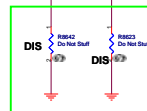


Under GPU.

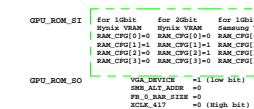


X7R, Under GPU.

Title		
Size	Document Number	Rev
Date:	Sheet	

[illegible]

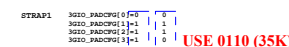
	Hynix 2G 0110 128*16*8 800MHz	Hynix 1G 0000 64*16*8 800MHz	Samsung 1G 0011 64*16*8 800MHz	Samsung 512 64*16*4 800MHz	Samsung 2G 0111 128*16*8 800MHz
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL



```

[ for 2Gbit
Samsung VRAM
1 RAM_CFG[0]=1
RAM_CFG[1]=1
0 RAM_CFG[2]=1
0 RAM_CFG[3]=0
]

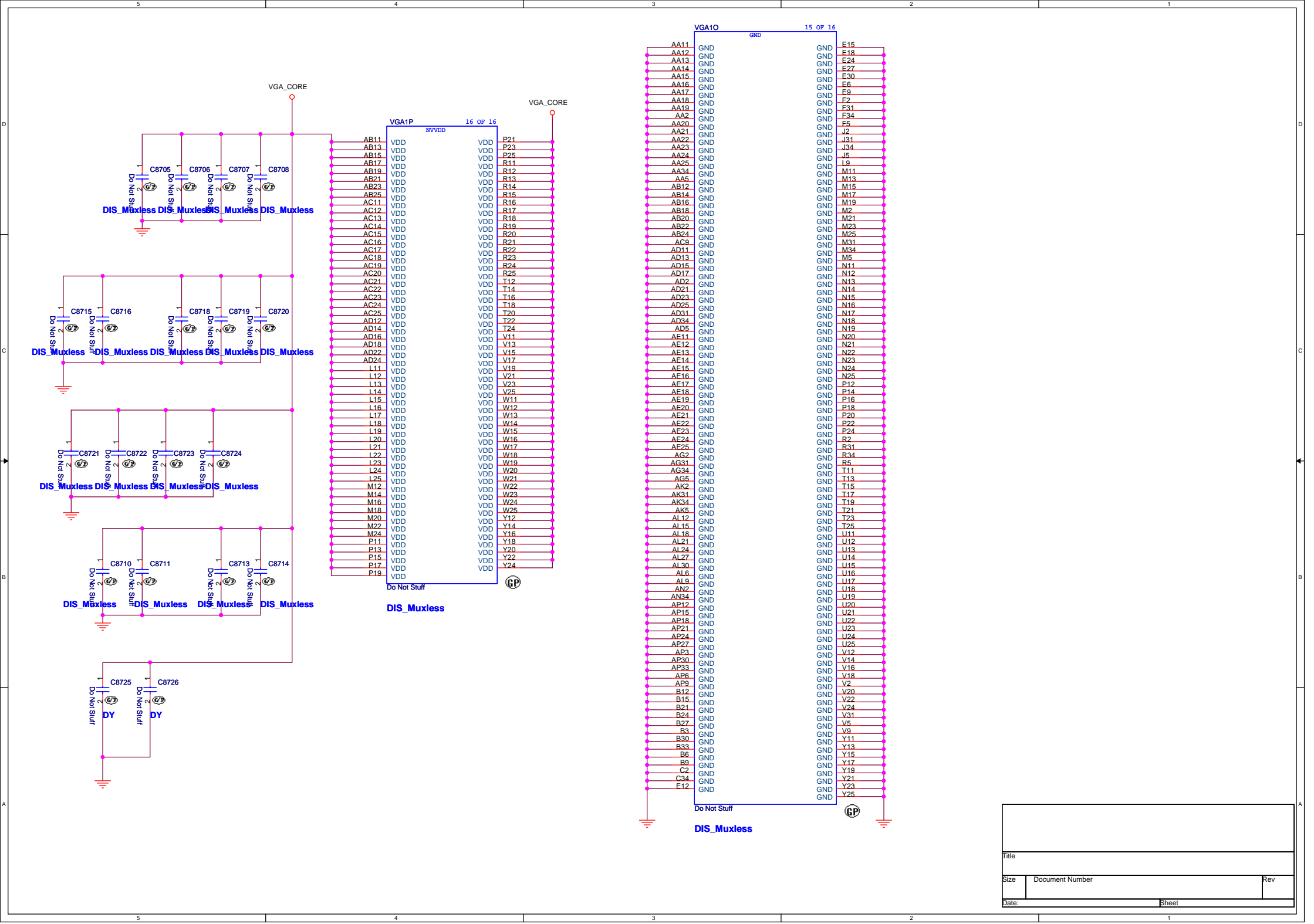
```

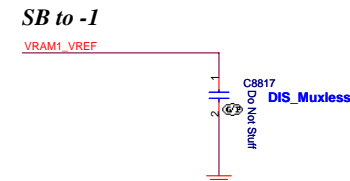
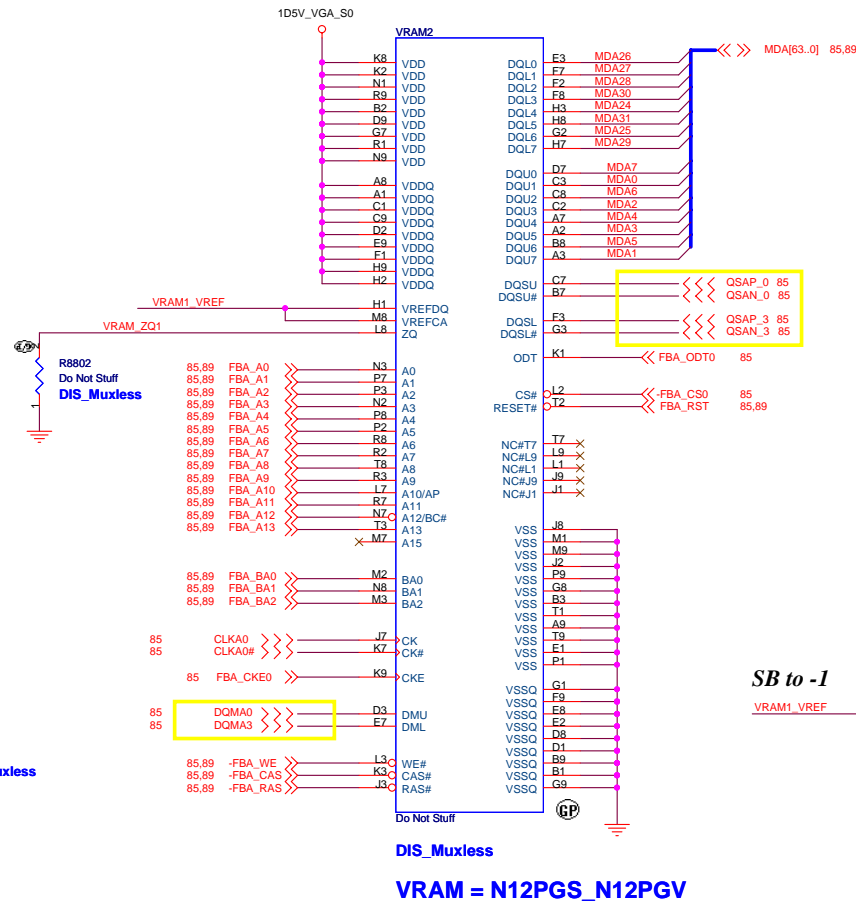
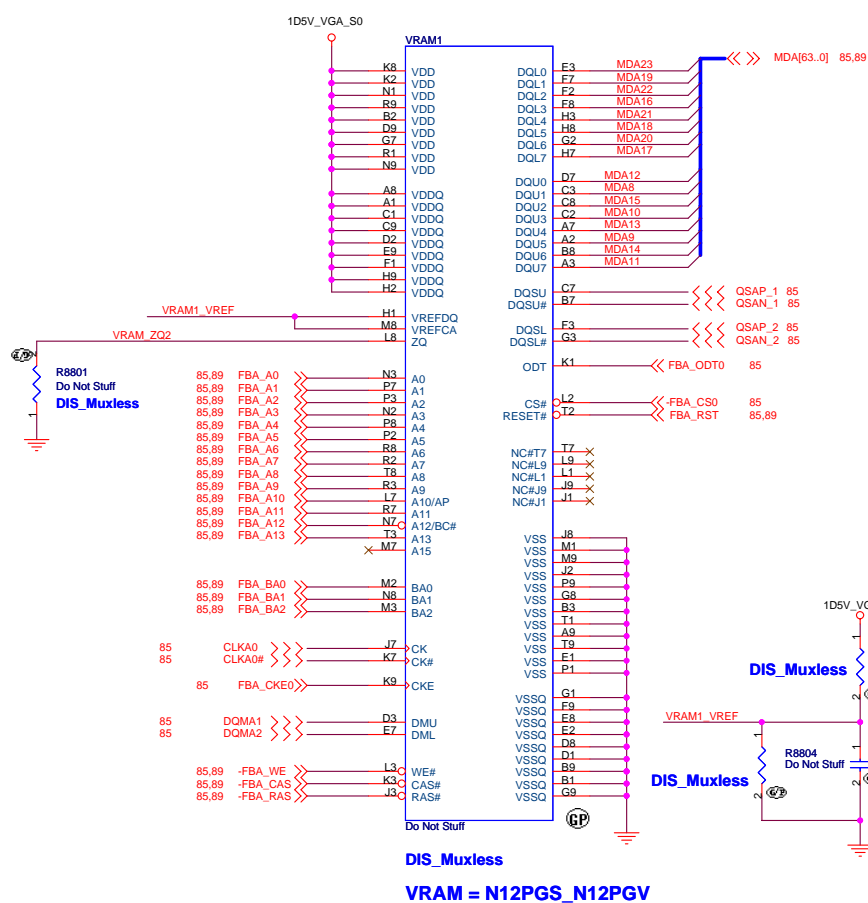


3

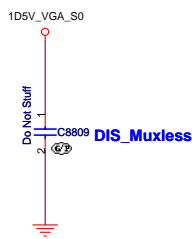
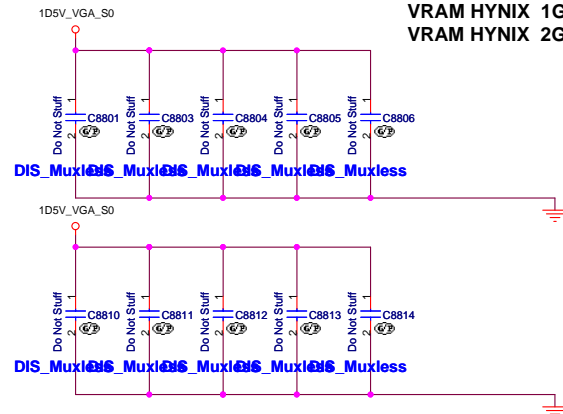
100

WWW.AliSaler.Com

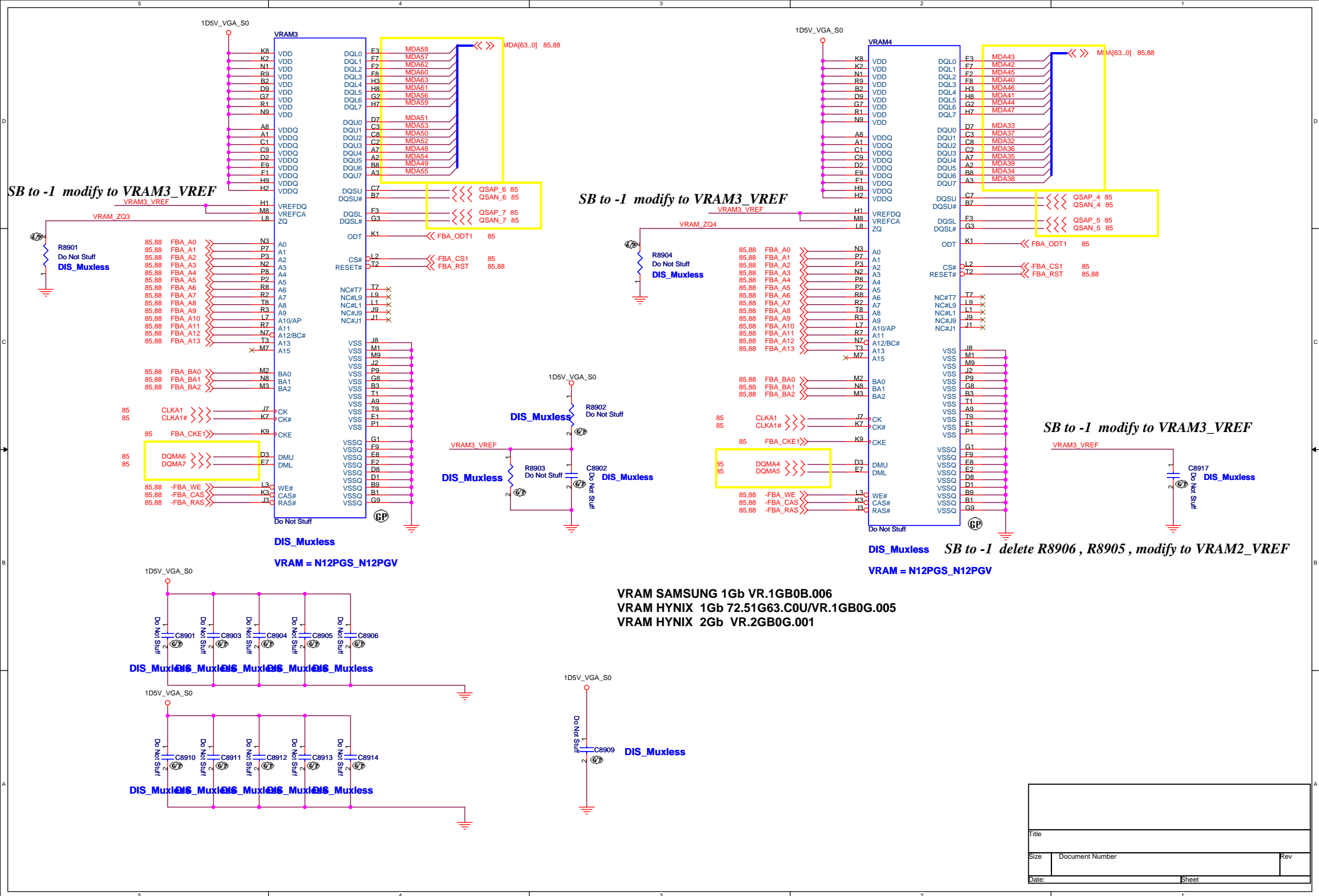


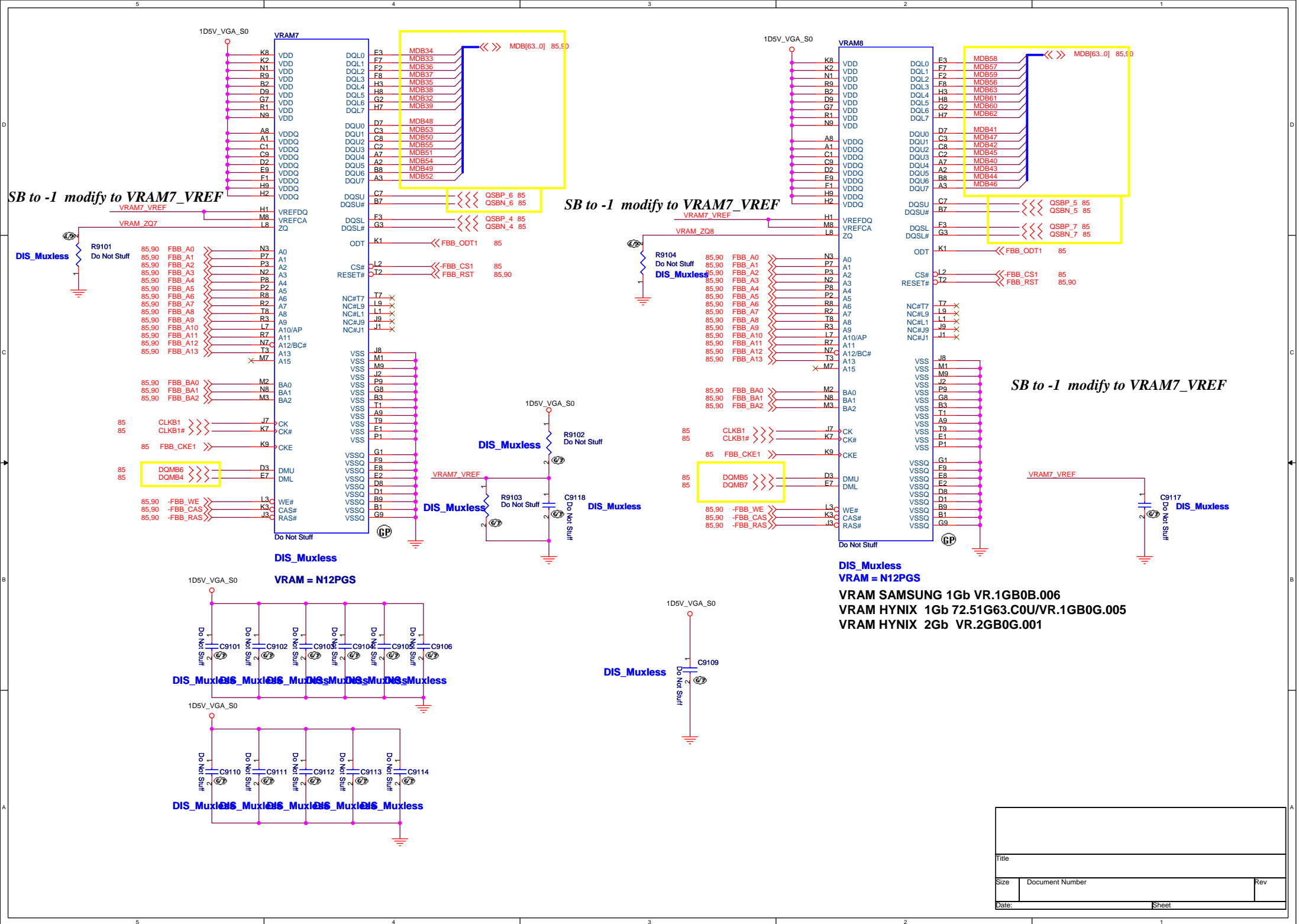


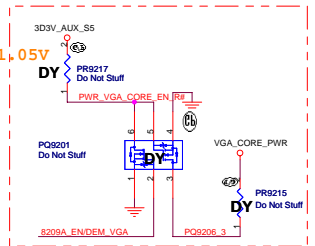
VRAM SAMSUNG 1Gb VR.1GB0B.006
 VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
 VRAM HYNIX 2Gb VR.2GB0G.001



Title		
Size	Document Number	Rev
Date	Sheet	

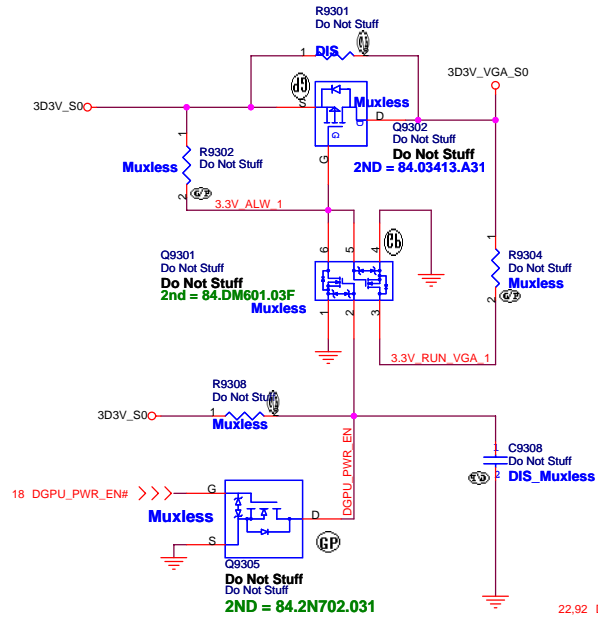




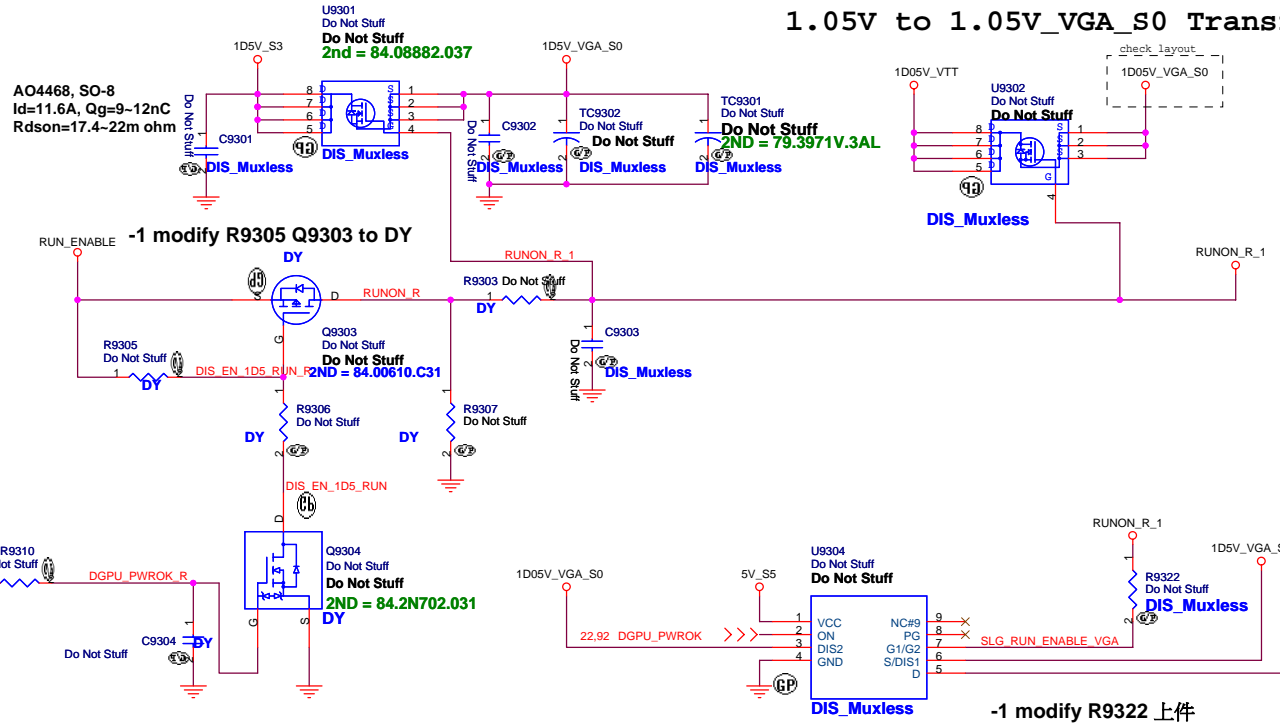


N12P GV			
P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

+3VS to 3.3V_DELAY Transfer

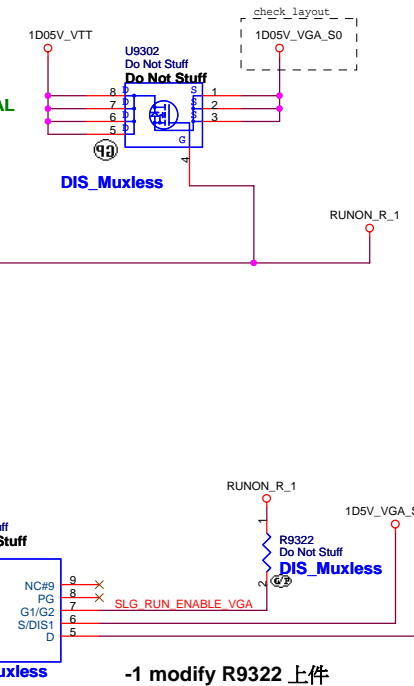


1D5V_VGA_S0

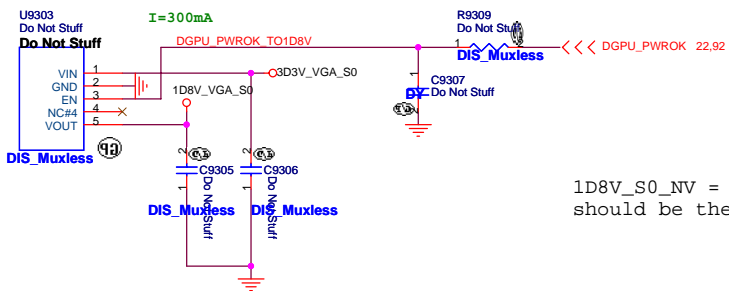


SB modify to 84.03006.A37

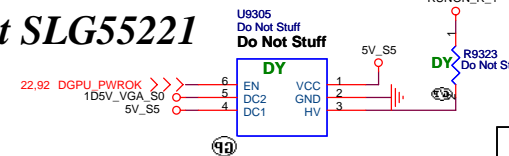
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer

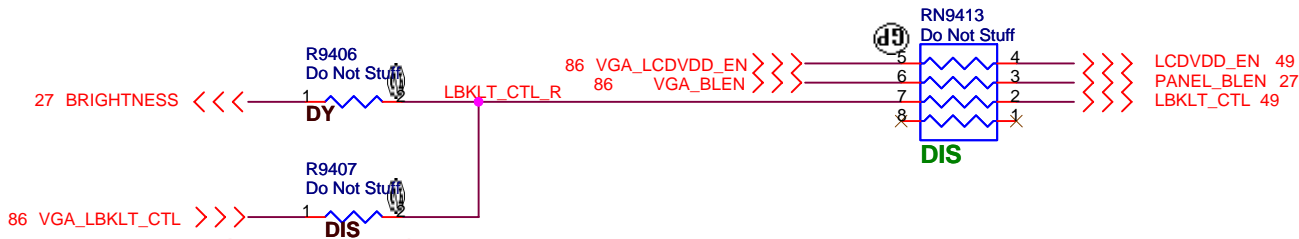
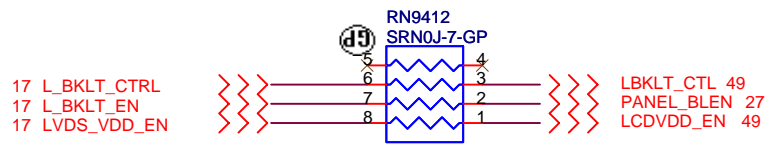
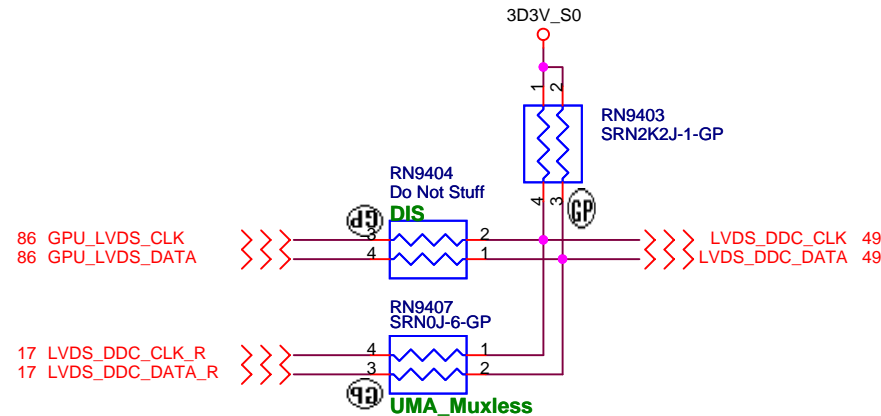
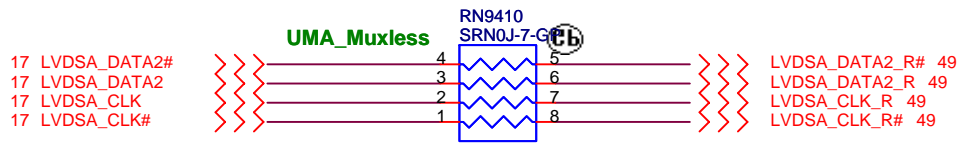
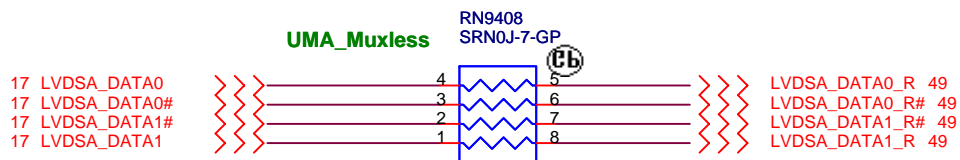
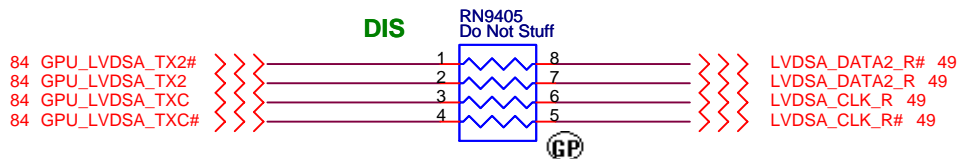
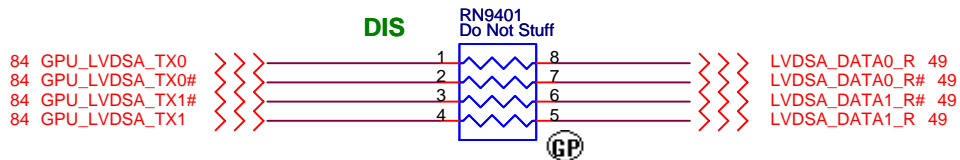


-1 co-layout SLG55221

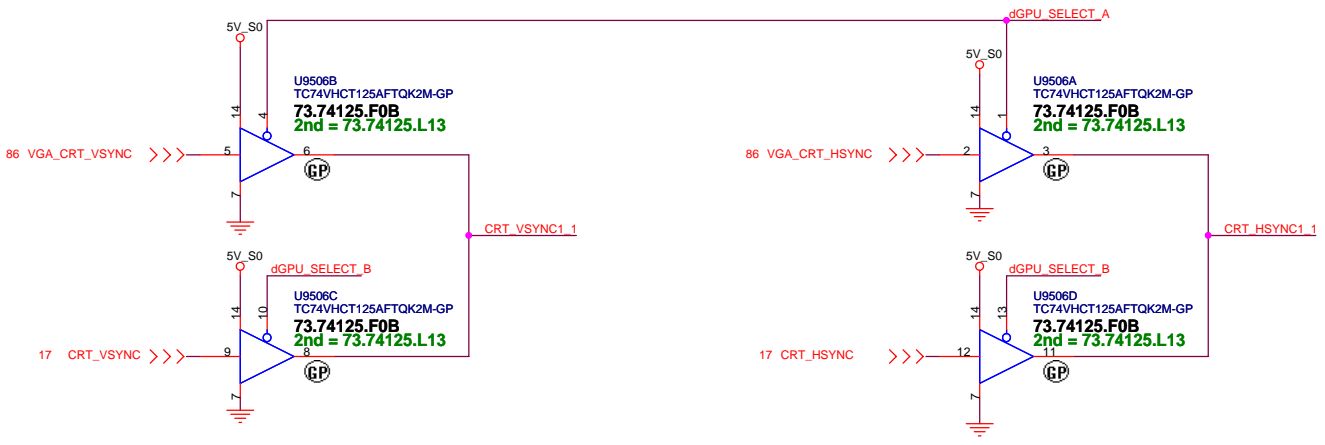
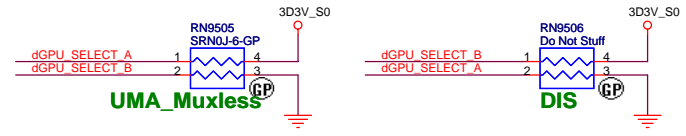
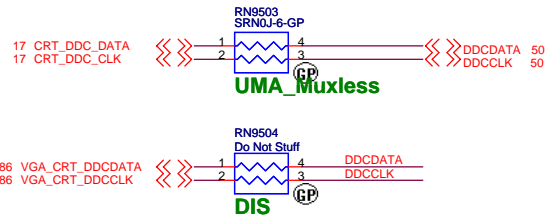
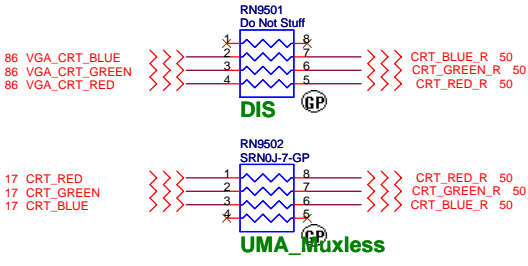


1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

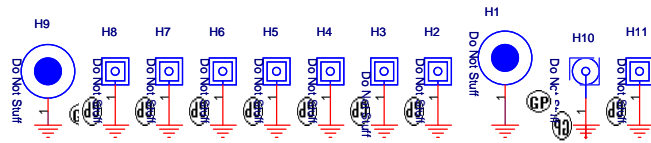
Title		
Size	Document Number	Rev
Date:	Sheet	



Title		
Size	Document Number	Rev
Date:	Sheet	

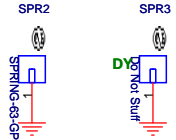


Title		
Size	Document Number	Rev
Date:	Sheet	

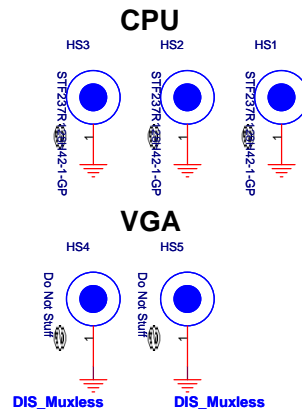
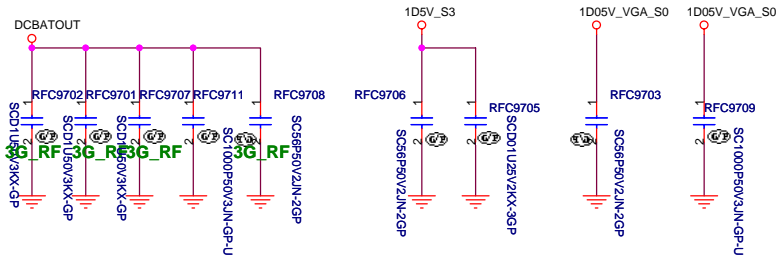
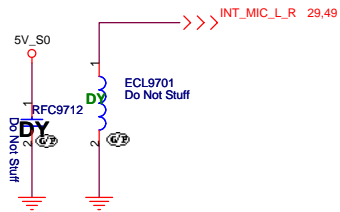
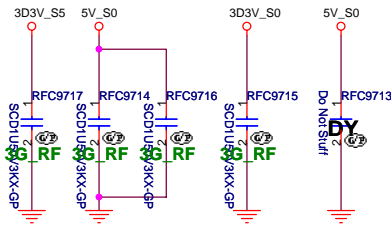


SB to -1 BOM add SPR2

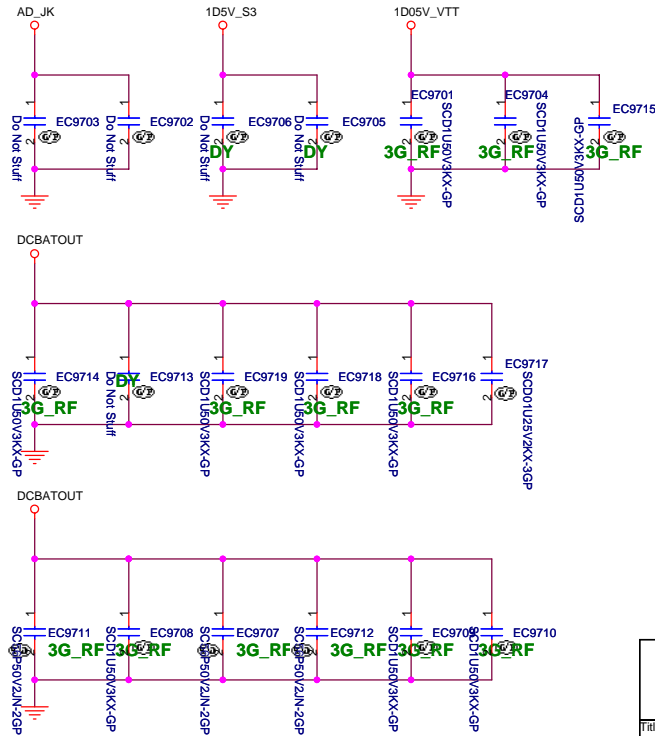
-2 delete SPR5



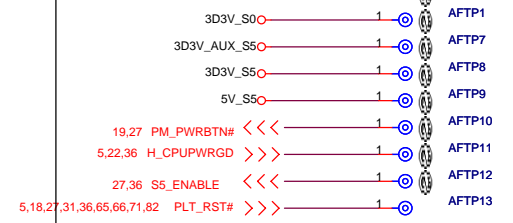
Change:34.40V16.001



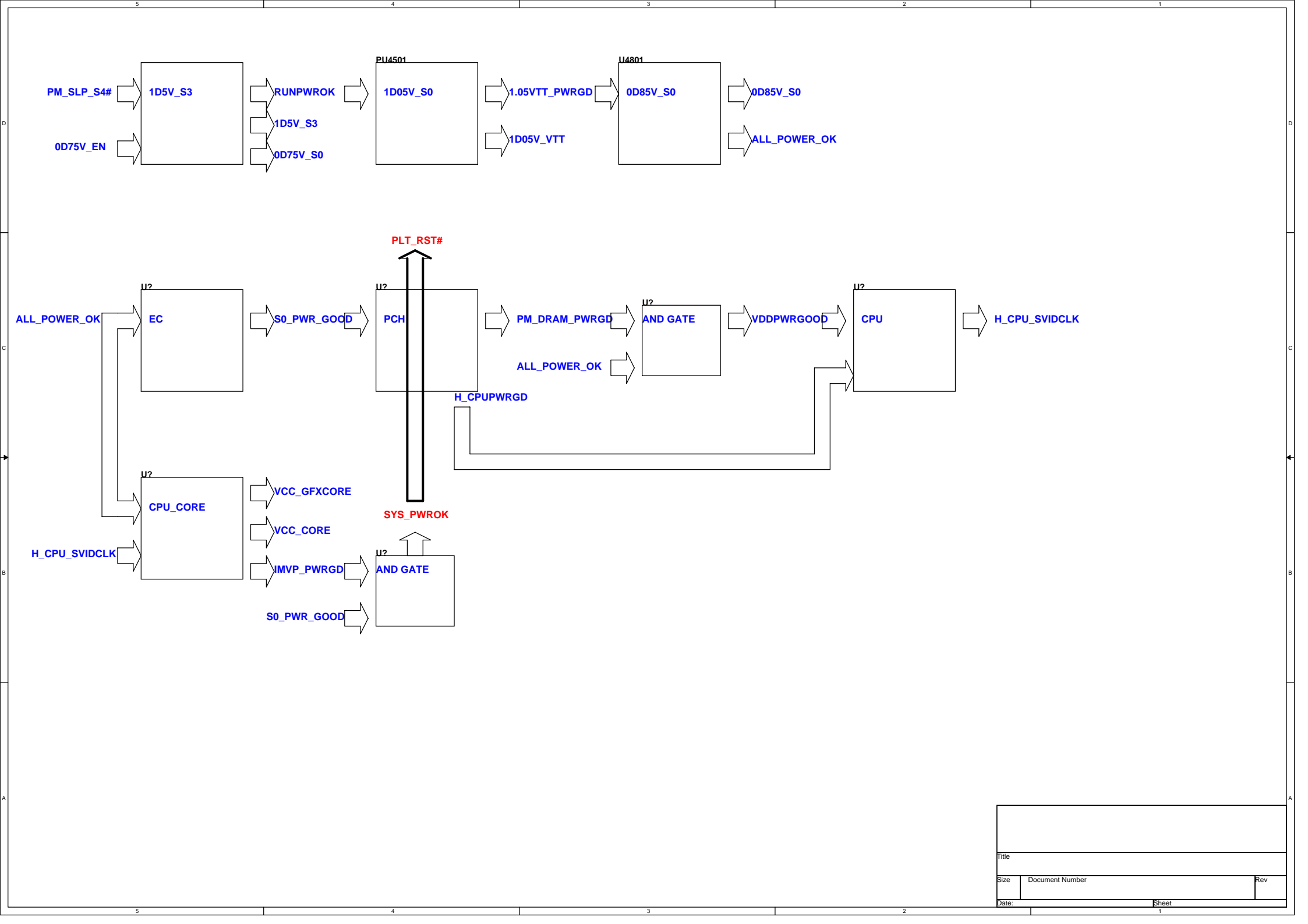
3G Sku



Check test point

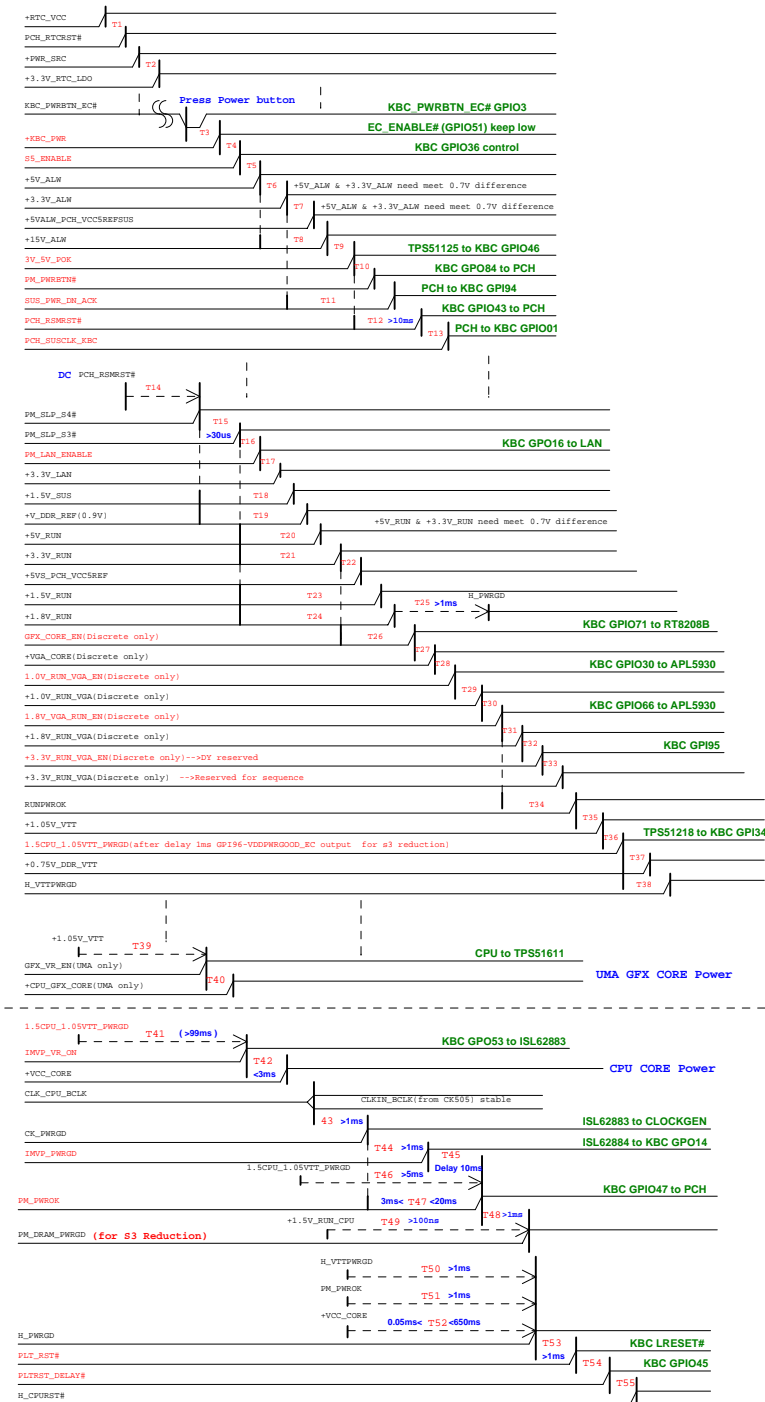


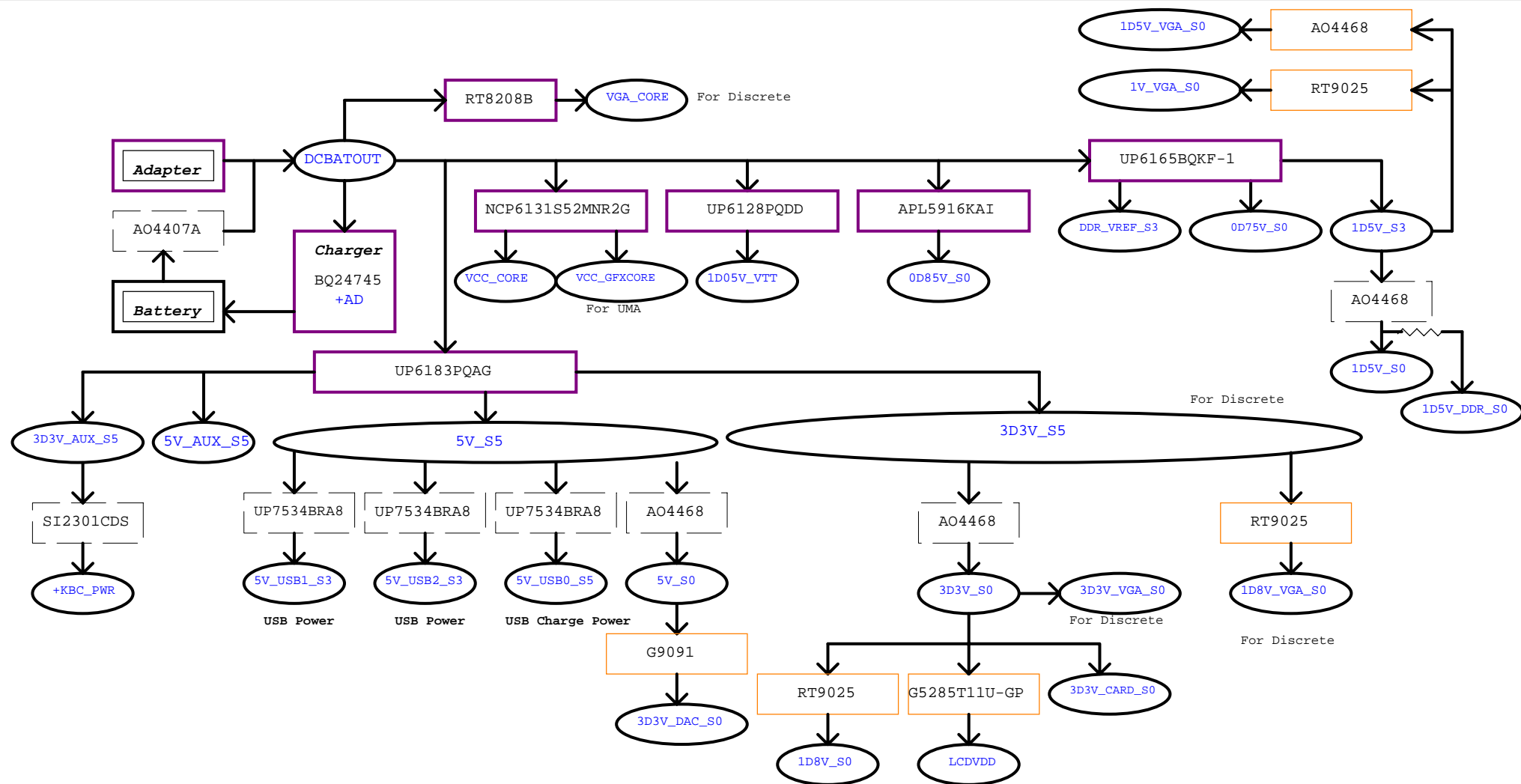
Test Point放在Dimm Door打開可量測處



(AC mode)

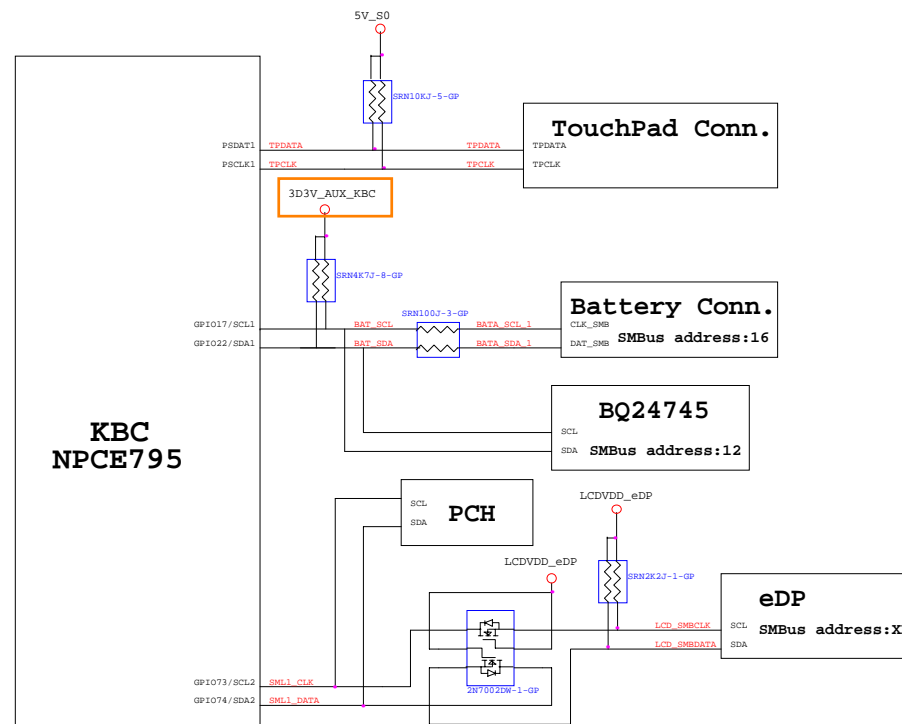
red word: KBC GPIO



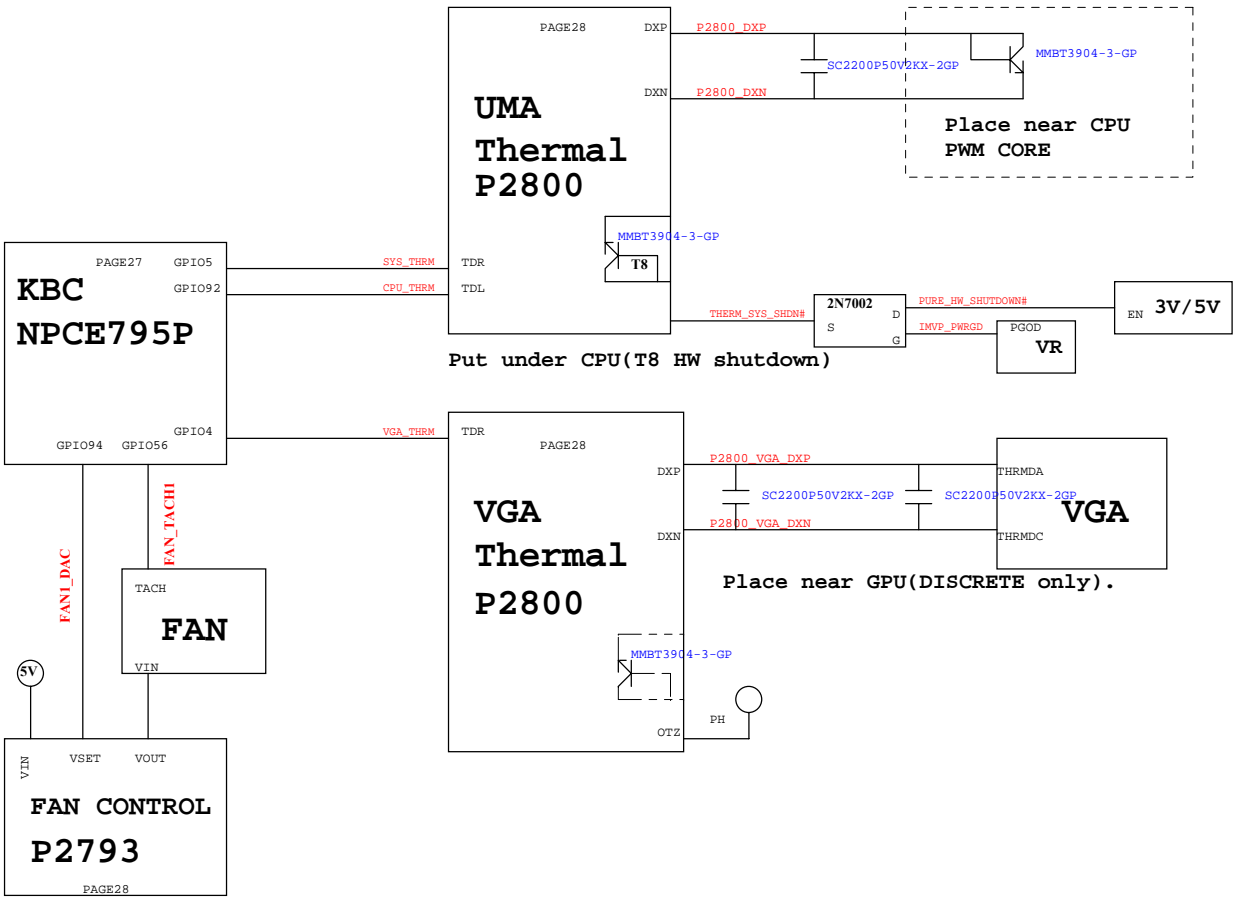


Title	
Size	Document Number
Date:	Sheet

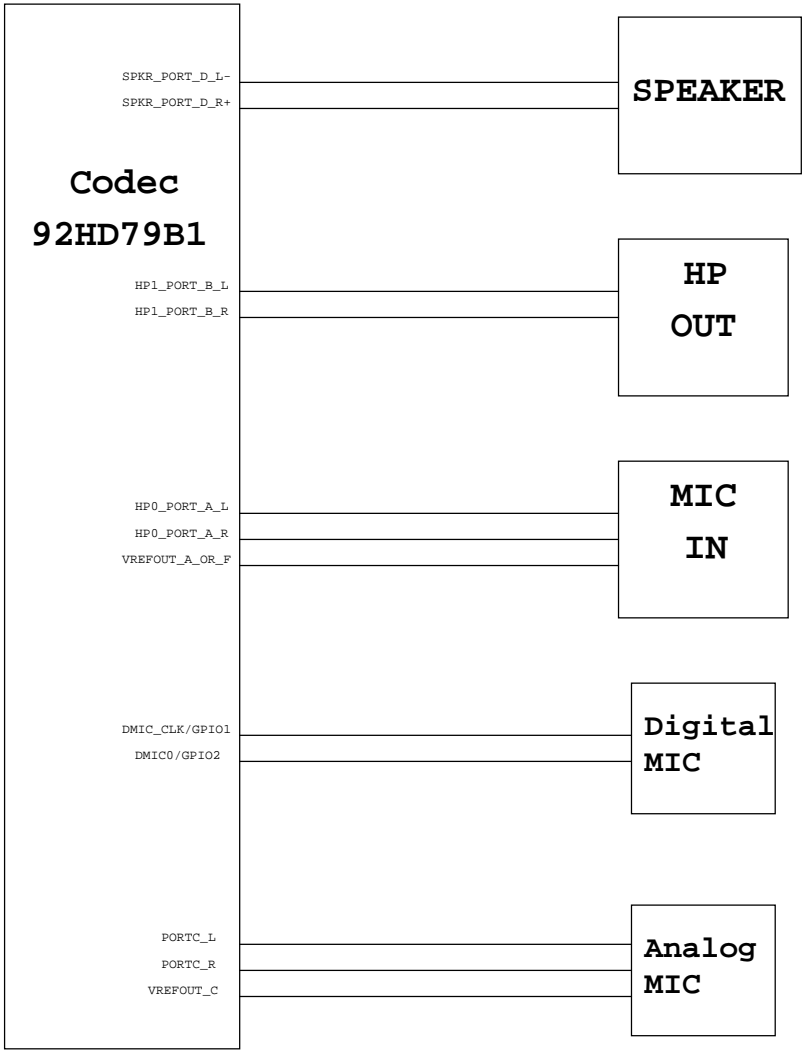
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Title		
Size	Document Number	Rev
Date:	Sheet	